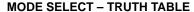
Dual D-Type Positive Edge-Triggered Flip-Flop

The SN74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and \overline{Q} outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.



OPERATING MODE		INPUTS	OUTPUTS		
OPERATING WIDDE	S _D	CD	D	ď	Q
Set	L	Н	Х	Н	L
Reset (Clear)	Н	L	Х	L	Н
*Undetermined	L	L	Χ	Н	Н
Load "1" (Set)	Н	Н	h	Н	L
Load "0" (Reset)	Н	Н	I	L	Н

* Both outputs will be HIGH while both \overline{S}_D and \overline{C}_D are LOW, but the output states are unpredictable if \overline{S}_D and \overline{C}_D go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

H, h = HIGH Voltage Level

L, I = LOW Voltage Level

X = Don't Care

I, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.



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LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 646



SOIC D SUFFIX CASE 751A



SOEIAJ M SUFFIX CASE 965

GUARANTEED OPERATING RANGES

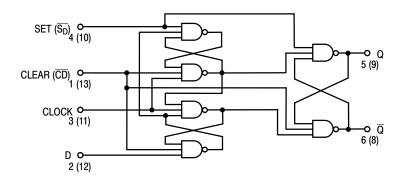
Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			-0.4	mA
I _{OL}	Output Current – Low			8.0	mA

ORDERING INFORMATION

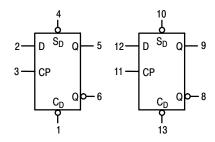
Device	Package	Shipping
SN74LS74AN	14 Pin DIP	2000 Units/Box
SN74LS74AD	SOIC-14	55 Units/Rail
SN74LS74ADR2	SOIC-14	2500/Tape & Reel
SN74LS74AM	SOEIAJ-14	See Note 1
SN74LS74AMEL	SOEIAJ-14	See Note 1

 For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

LOGIC DIAGRAM (Each Flip-Flop)



LOGIC SYMBOL



V_{CC} = PIN 14 GND = PIN 7

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Co	onditions
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input All Inputs	HIGH Voltage for
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input All Inputs	LOW Voltage for
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -	-18 mA
V _{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = MIN, I_{OH} =$ or V_{IL} per Truth Ta	
.,			0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$
V_{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 8.0 mA	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table
l _{IH}	Input High Current Data, Clock Set, Clear			20 40	μΑ	V _{CC} = MAX, V _{IN} =	= 2.7 V
""	Data, Clock Set, Clear			0.1 0.2	mA	V _{CC} = MAX, V _{IN} =	= 7.0 V
I _{IL}	Input LOW Current Data, Clock Set, Clear			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} =	= 0.4 V
I _{OS}	Output Short Circuit Current (Note 2)	-20		-100	mA	V _{CC} = MAX	
Icc	Power Supply Current			8.0	mA	V _{CC} = MAX	

^{2.} Not more than one output should be shorted at a time, nor for more than 1 second.

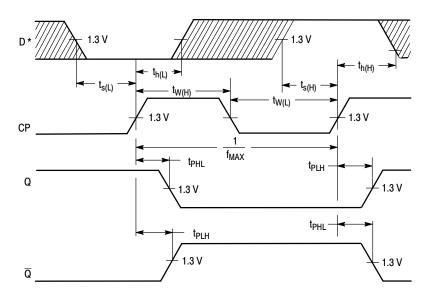
AC CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$)

			Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Co	onditions
f _{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	
t _{PLH}	Olarida Olaras Ontara Ontarat		13	25	ns	Fig	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 15 \text{ pF}$
t _{PHL}	Clock, Clear, Set to Output		25	40	ns	Figure 1	οι – 10 βι

AC SETUP REQUIREMENTS $(T_A = 25^{\circ}C)$

		Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Test Co	onditions
t _{W(H)}	Clock	25			ns	Figure 1	
t _{W(L)}	Clear, Set	25			ns	Figure 2	
	Data Setup Time — HIGH	20			ns	Figure 4	V _{CC} = 5.0 V
t _s	LOW	20			ns	Figure 1	
t _h	Hold Time	5.0			ns	Figure 1	

AC WAVEFORMS



^{*}The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width

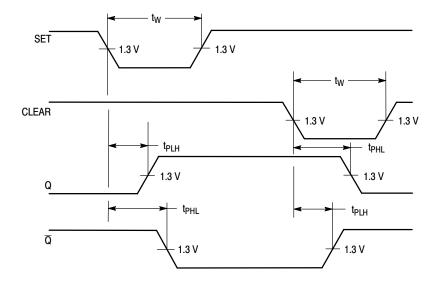
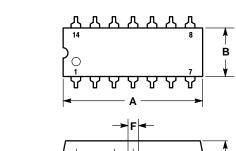
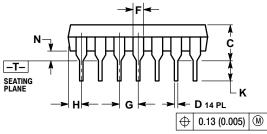


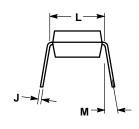
Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths

PACKAGE DIMENSIONS

N SUFFIX PLASTIC PACKAGE CASE 646-06 ISSUE M





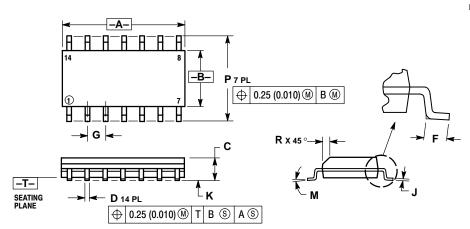


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	METERS		
DIM	MIN	MAX	MIN	MAX		
Α	0.715	0.770	18.16	18.80		
В	0.240	0.260	6.10	6.60		
С	0.145	0.185	3.69	4.69		
D	0.015	0.021	0.38	0.53		
F	0.040	0.070	1.02	1.78		
G	0.100	BSC	2.54 BSC			
Н	0.052	0.095	1.32	2.41		
J	0.008	0.015	0.20	0.38		
K	0.115	0.135	2.92	3.43		
L	0.290	0.310	7.37	7.87		
M		10°		10°		
N	0.015	0.039	0.38	1.01		

PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

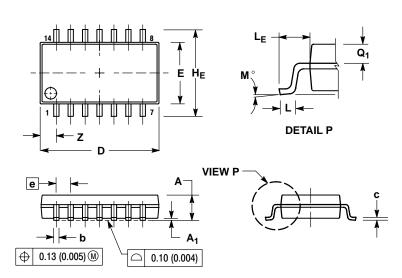
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	8.55	8.75	0.337	0.344	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
7	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0 °	7°	0°	7°	
P	5.80	6.20	0.228	0.244	
R	0.25	0.50	0.010	0.019	

PACKAGE DIMENSIONS

M SUFFIX

SOEIAJ PACKAGE CASE 965-01 **ISSUE O**



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A ₁	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	9.90	10.50	0.390	0.413	
Е	5.10	5.45	0.201	0.215	
е	1.27	1.27 BSC		BSC	
HE	7.40	8.20	0.291	0.323	
0.50	0.50	0.85	0.020	0.033	
F	1.10	1.50	0.043	0.059	
M	0 °	10°	0 °	10 °	
Q ₁	0.70	0.90	0.028	0.035	
Z		1.42		0.056	

SN741 S74A

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