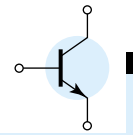


CHAPTER

DC Biasing—BJTs 4

4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the BJT amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point—a number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations—another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$V_{BE} = 0.7 \text{ V} \tag{4.1}$$

$$I_E = (\beta + 1)I_B \cong I_C \tag{4.2}$$

$$I_C = \beta I_B \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a num-

ber of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\ \mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{sat}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, one can select many different operating areas or points. The chosen *Q*-point often depends on the intended use of the circuit. Still, we can consider some differences among the

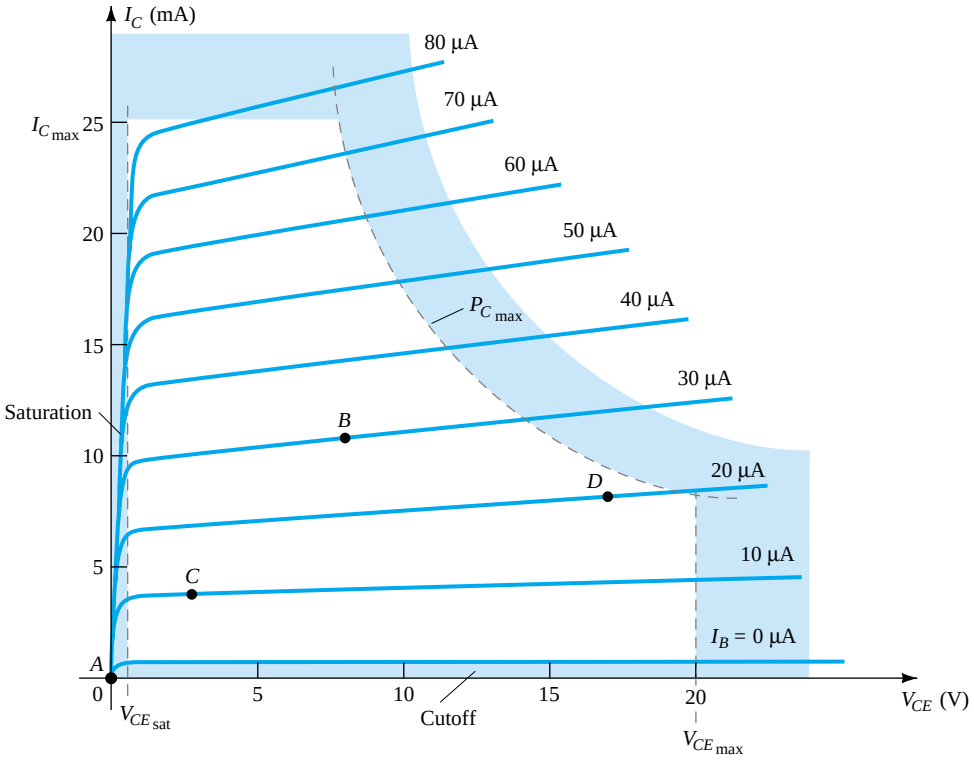
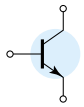


Figure 4.1 Various operating points within the limits of operation of a transistor.



various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at *A*—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point *A* would not be suitable. For point *B*, if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cutoff* or *saturation*. Point *C* would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0\text{V}/I_C = 0$ mA. Operating at point *C* also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point *B* is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point *D* sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point *B* therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 8) but not the case necessarily for power amplifiers, which will be considered in Chapter 16. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor*, *S*, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base–emitter junction *must* be forward-biased (*p*-region voltage more *p*ositive), with a resulting forward-bias voltage of about 0.6 to 0.7 V.
2. The base–collector junction *must* be reverse-biased (*n*-region more *p*ositive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the *p*-*n* junction is *p*-*p*ositive, while for reverse bias it is opposite (reverse) with *n*-*p*ositive. This emphasis on the initial letter should provide a means of helping memorize the necessary voltage polarity.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base–emitter junction forward biased
   Base–collector junction reverse biased

2. *Cutoff-region operation:*
   Base–emitter junction reverse biased
3. *Saturation-region operation:*
   Base–emitter junction forward biased
   Base–collector junction forward biased

4.3 FIXED-BIAS CIRCUIT

The fixed-bias circuit of Fig. 4.2 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

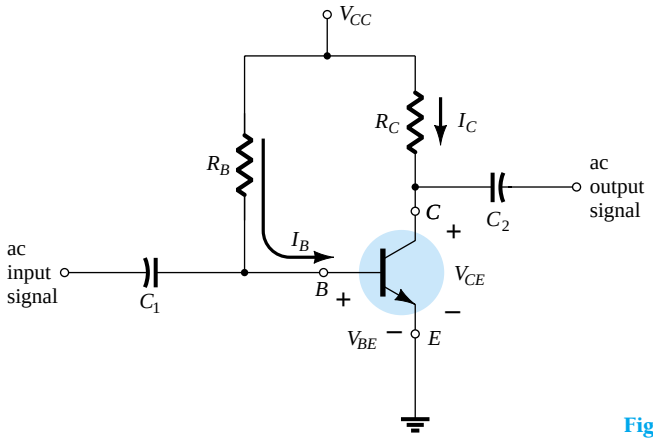


Figure 4.2 Fixed-bias circuit.

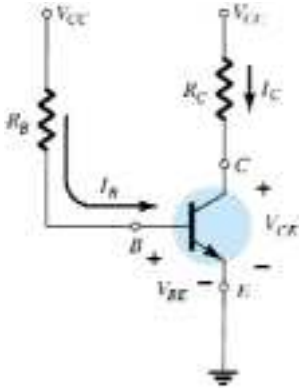


Figure 4.3 dc equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}).

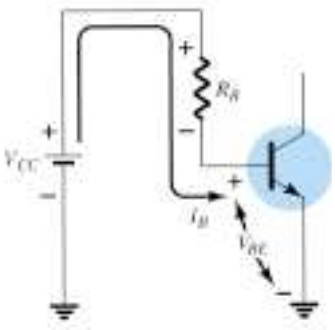


Figure 4.4 Base–emitter loop.

In addition, since the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor, R_B, sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B \tag{4.5}$$

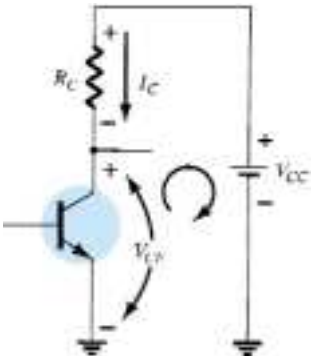


Figure 4.5 Collector–emitter loop.

It is interesting to note that since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Change R_C to any level and it will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 will result in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C R_C \tag{4.6}$$

which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground respectively. But *in this case*, since $V_E = 0$ V, we have

$$V_{CE} = V_C \tag{4.8}$$

In addition, since

$$V_{BE} = V_B - V_E \tag{4.9}$$

and $V_E = 0$ V, then

$$V_{BE} = V_B \tag{4.10}$$

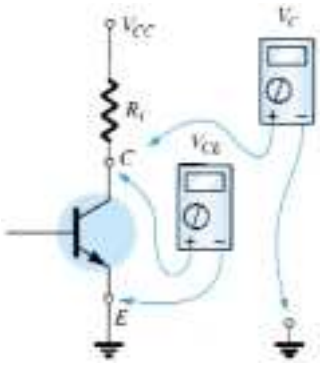


Figure 4.6 Measuring V_{CE} and V_C.

Keep in mind that voltage levels such as V_{CE} are determined by placing the red (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

EXAMPLE 4.1

Determine the following for the fixed-bias configuration of Fig. 4.7.

(a) I_{B_Q} and I_{C_Q}.
(b) V_{CE_Q}.
(c) V_B and V_C.
(d) V_{BC}.

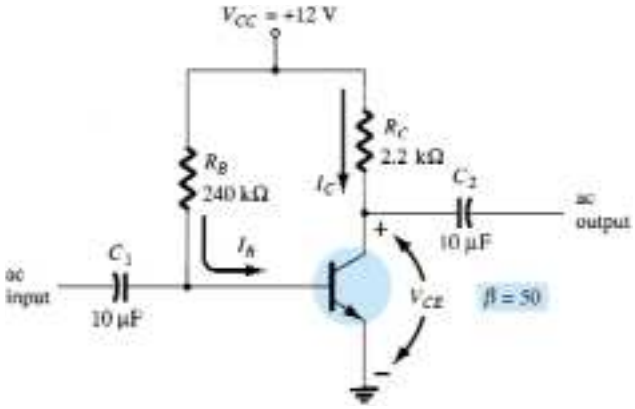


Figure 4.7 dc fixed-bias circuit for Example 4.1.

Solution

(a) Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

(b) Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

(c) $V_B = V_{BE} = \mathbf{0.7\ V}$

$V_C = V_{CE} = \mathbf{6.83\ V}$

(d) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high and the voltage V_{CE} is assumed to be zero volts. Applying Ohm's law the resistance between collector and emitter terminals can be determined as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

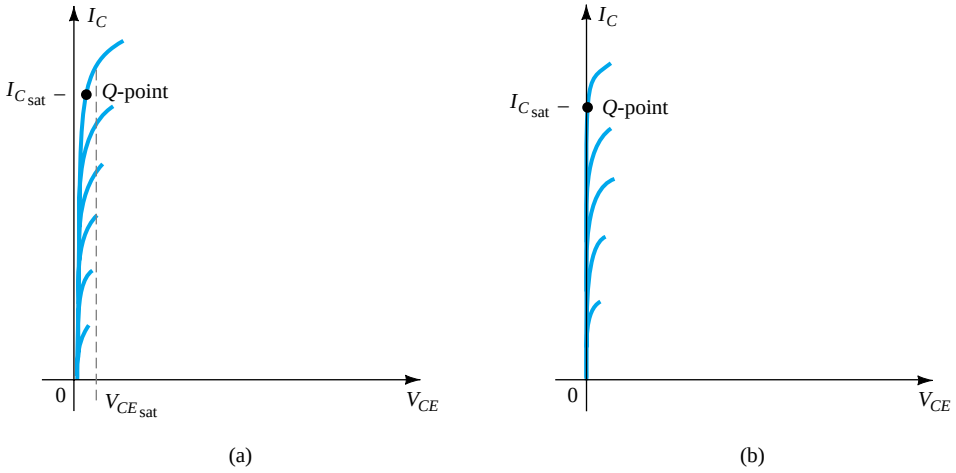


Figure 4.8 Saturation regions: (a) actual; (b) approximate.

Applying the results to the network schematic would result in the configuration of Fig. 4.9.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

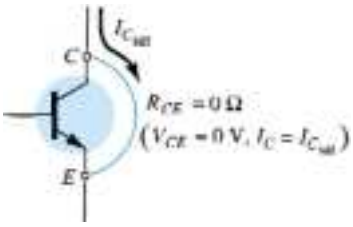


Figure 4.9 Determining $I_{C_{sat}}$.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.11}$$

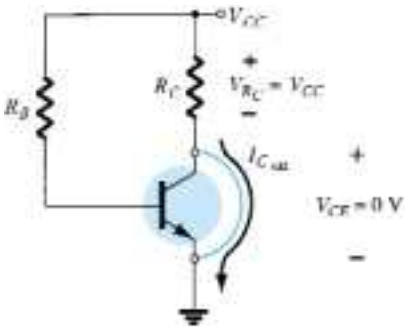


Figure 4.10 Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once $I_{C_{sat}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2

Determine the saturation level for the network of Fig. 4.7.

Solution

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\ \text{V}}{2.2\ \text{k}\Omega} = \mathbf{5.45\ mA}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

The analysis thus far has been performed using a level of β corresponding with the resulting Q-point. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

In essence, therefore, we have a network equation and a set of characteristics that employ the same variables. The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$V_{CE} = V_{CC}\,|_{I_C = 0\text{ mA}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

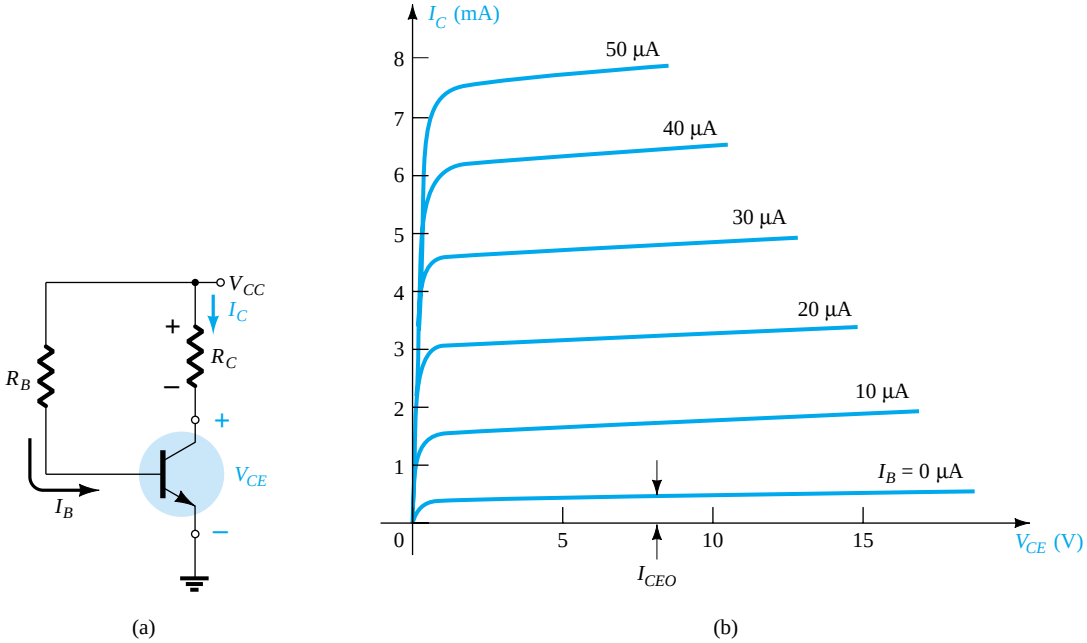


Figure 4.11 Load-line analysis: (a) the network; (b) the device characteristics.

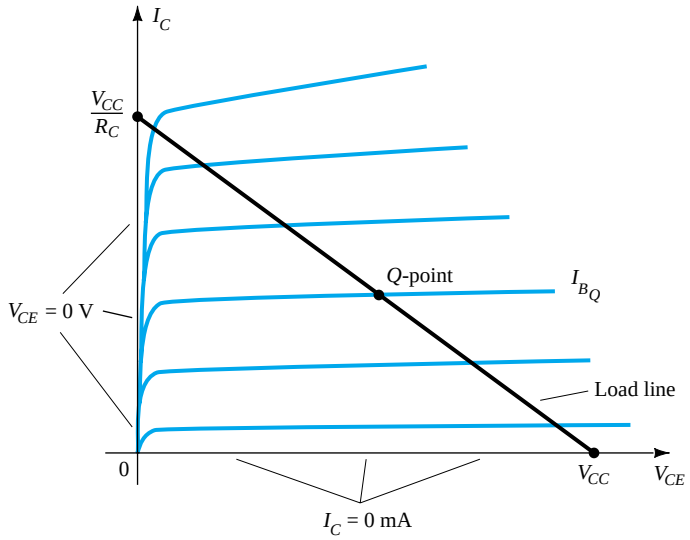


Figure 4.12 Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE} = 0\text{ V}}} \tag{4.14}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), the straight line established by Eq. (4.12) can be drawn. The resulting line on the graph of Fig. 4.12 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, the actual Q-point can be established as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B the Q-point moves up or down the load line as shown in Fig. 4.13. If V_{CC} is held fixed and R_C changed, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} varied, the load line shifts as shown in Fig. 4.15.

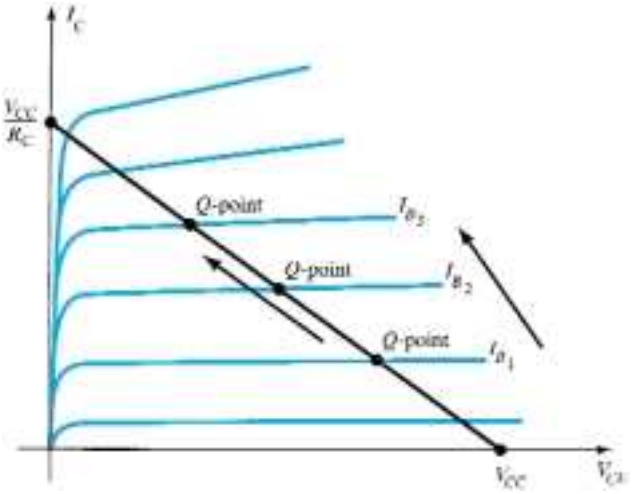


Figure 4.13 Movement of Q-point with increasing levels of I_B.

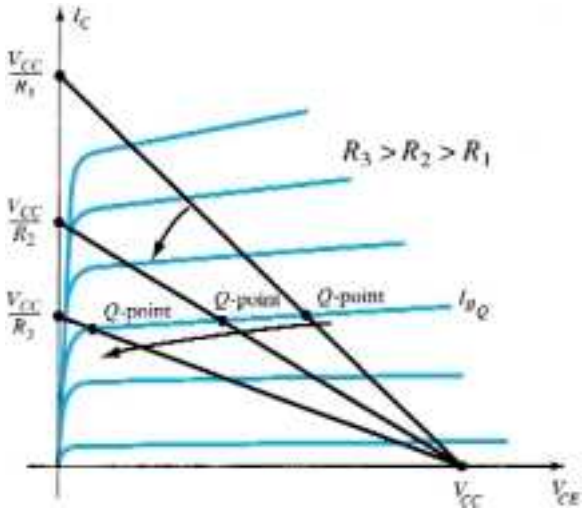


Figure 4.14 Effect of increasing levels of R_C on the load line and Q-point.

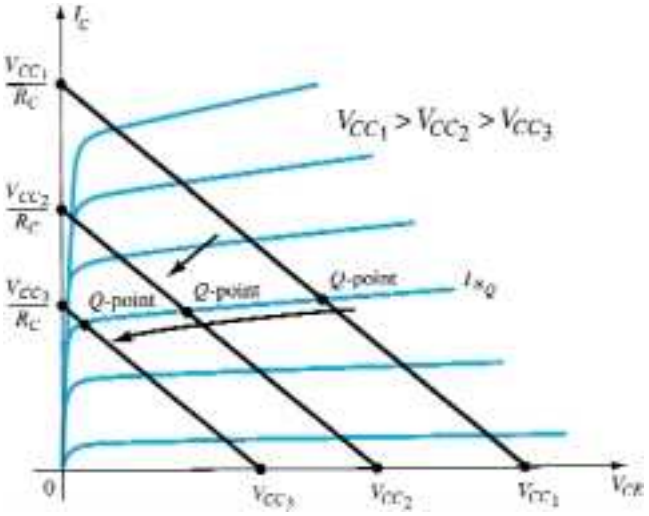


Figure 4.15 Effect of lower values of V_{CC} on the load line and Q-point.

EXAMPLE 4.3

Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

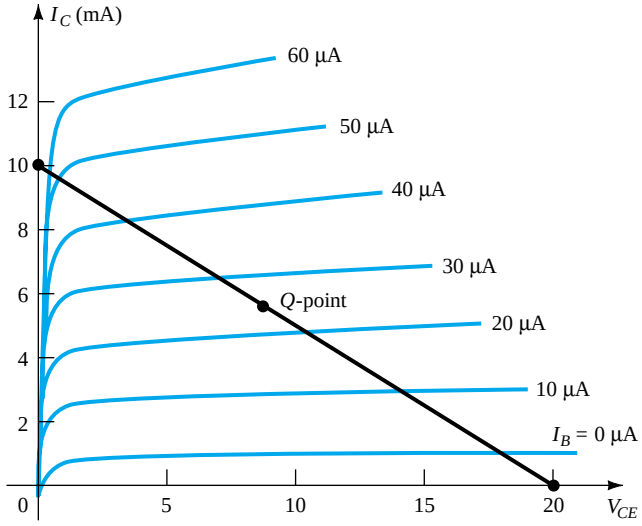


Figure 4.16 Example 4.3

Solution

From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

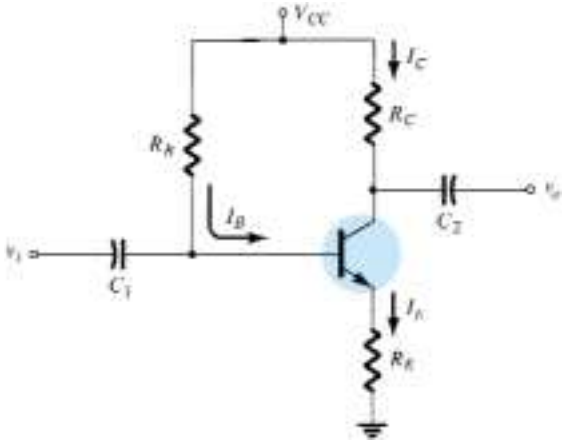


Figure 4.17 BJT bias circuit with emitter resistor.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.17 can be redrawn as shown in Fig. 4.18. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \tag{4.15}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \tag{4.16}$$

Substituting for I_E in Eq. (4.15) will result in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms will then provide the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1) we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.17}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is

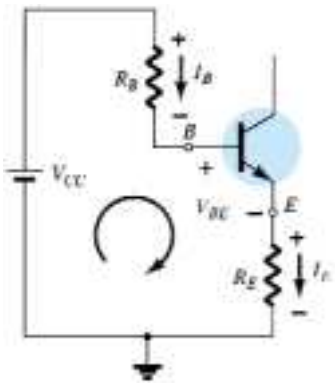


Figure 4.18 Base–emitter loop.

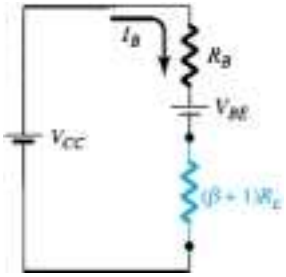


Figure 4.19 Network derived from Eq. (4.17).

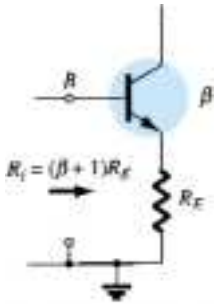


Figure 4.20 Reflected impedance level of R_E.

the case for the network of Fig. 4.19. Solving for the current I_B will result in the same equation obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base–emitter loop. Since β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.20,

$$R_i = (\beta + 1)R_E \tag{4.18}$$

Equation (4.18) is one that will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base–emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

Collector–Emitter Loop

The collector–emitter loop is redrawn in Fig. 4.21. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.19}$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \tag{4.20}$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \tag{4.21}$$

or

$$V_C = V_{CC} - I_C R_C \tag{4.22}$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B \tag{4.23}$$

or

$$V_B = V_{BE} + V_E \tag{4.24}$$

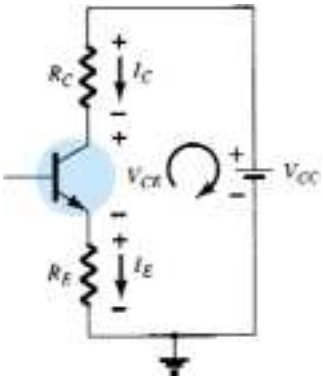


Figure 4.21 Collector–emitter loop.

EXAMPLE 4.4

For the emitter bias network of Fig. 4.22, determine:

(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.
(e) V_E.
(f) V_B.
(g) V_{BC}.

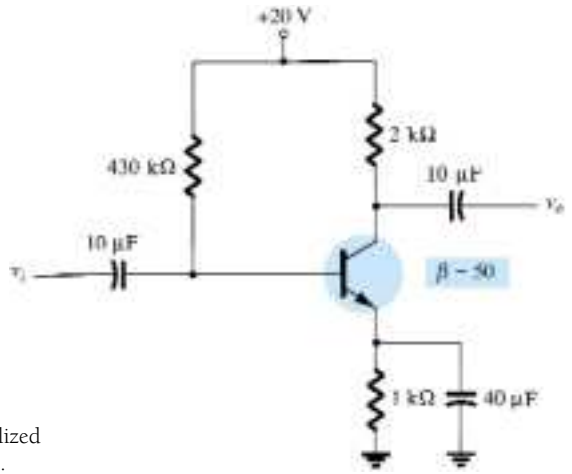


Figure 4.22 Emitter-stabilized bias circuit for Example 4.4.

Solution

(a) Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

(c) Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\ V}$

(d) $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\ V}$

(e) $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\ V}$

(f) $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\ V}$

(g) $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\ V}$ (reverse-biased as required)

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change. While a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5

Prepare a table and compare the bias voltage and currents of the circuits of Figs. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution

Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. I_B is the same and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C—or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in β.

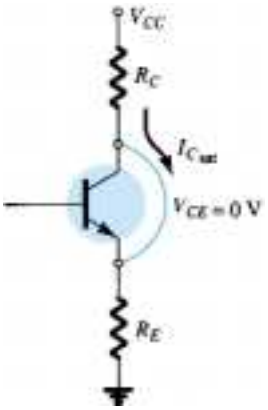


Figure 4.23 Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \tag{4.25}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

Determine the saturation current for the network of Example 4.4.

EXAMPLE 4.6

Solution

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$= \frac{20\ \text{V}}{2\ \text{k}\Omega + 1\ \text{k}\Omega} = \frac{20\ \text{V}}{3\ \text{k}\Omega}$$

$$= \mathbf{6.67\ mA}$$

which is about twice the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.24 (denoted I_{B_Q}).

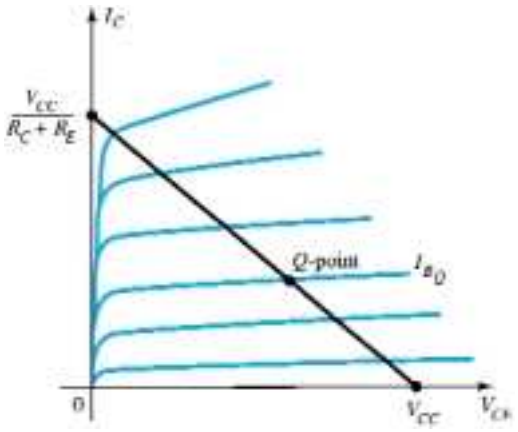


Figure 4.24 Load line for the emitter-bias configuration.

The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\ \text{V}}} \tag{4.27}$$

as shown in Fig. 4.24. Different levels of I_{B_Q} will, of course, move the *Q*-point up or down the load line.

4.5 VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in

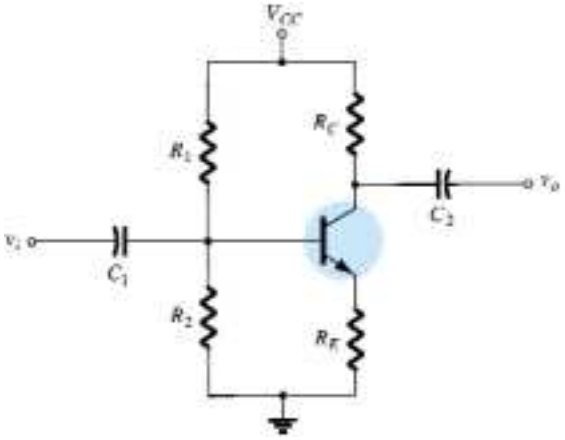


Figure 4.25 Voltage-divider bias configuration.

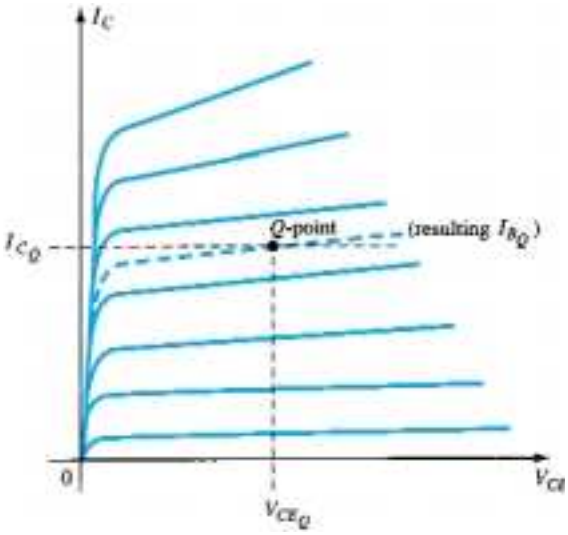


Figure 4.26 Defining the *Q*-point for the voltage-divider bias configuration.

fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a *Q*-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.26. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method* that can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

Exact Analysis

The input side of the network of Fig. 4.25 can be redrawn as shown in Fig. 4.27 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

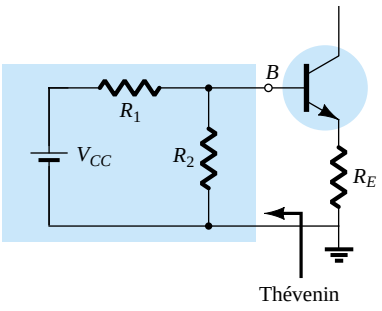


Figure 4.27 Redrawing the input side of the network of Fig. 4.25.

R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.28.

$$R_{Th} = R_1 \| R_2 \tag{4.28}$$

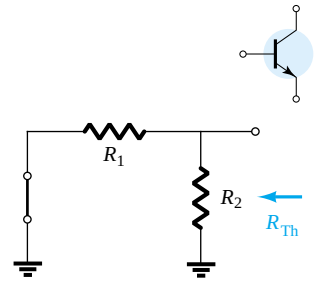


Figure 4.28 Determining R_{Th}.

E_{Th}: The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$

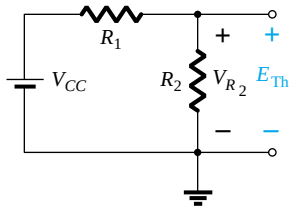


Figure 4.29 Determining E_{Th}.

The Thévenin network is then redrawn as shown in Fig. 4.30, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \tag{4.30}$$

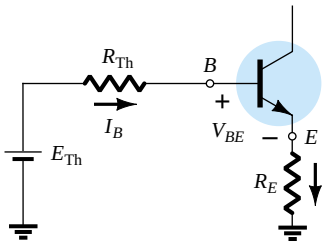


Figure 4.30 Inserting the Thévenin equivalent circuit.

Although Eq. (4.30) initially appears different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.31}$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

EXAMPLE 4.7

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.31.

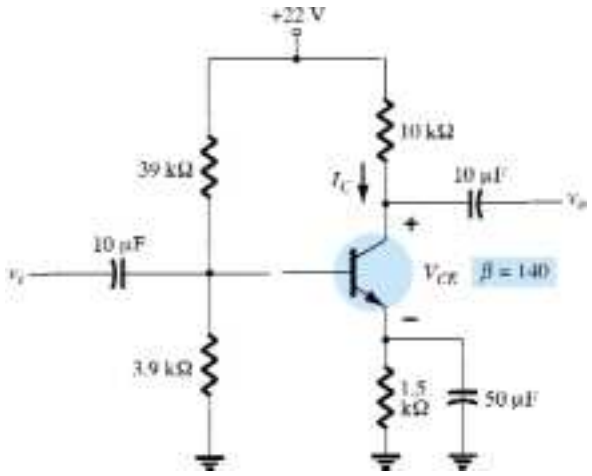


Figure 4.31 Beta-stabilized circuit for Example 4.7.

Solution

Eq. (4.28): $R_{Th} = R_1 \| R_2$

$$= \frac{(39\ \text{k}\Omega)(3.9\ \text{k}\Omega)}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 3.55\ \text{k}\Omega$$

Eq. (4.29): $$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ V$$

Eq. (4.30): $$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\ \text{V} - 0.7\ \text{V}}{3.55\ \text{k}\Omega + (141)(1.5\ \text{k}\Omega)} = \frac{1.3\ \text{V}}{3.55\ \text{k}\Omega + 211.5\ \text{k}\Omega}$$

$$= 6.05\ \mu A$$

$$I_C = \beta I_B$$

$$= (140)(6.05\ \mu\text{A})$$

$$= \mathbf{0.85\ mA}$$

Eq. (4.31): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\ \text{V} - (0.85\ \text{mA})(10\ \text{k}\Omega + 1.5\ \text{k}\Omega)$$

$$= 22\ \text{V} - 9.78\ \text{V}$$

$$= \mathbf{12.22\ V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then $I_1 = I_2$ and R_1 and R_2 can be considered series ele-

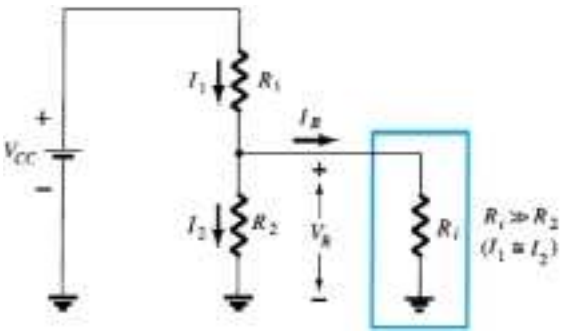


Figure 4.32 Partial-bias circuit for calculating the approximate base voltage V_B.

ments. The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.32}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2 \tag{4.33}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE} \tag{4.34}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \tag{4.35}$$

and

$$I_{C_Q} \cong I_E \tag{4.36}$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) \tag{4.37}$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{C_Q} and V_{CE_Q}) is therefore independent of the value of β.

EXAMPLE 4.8

Repeat the analysis of Fig. 4.31 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution

Testing:

$$\beta R_E \geq 10R_2$$

$$(140)(1.5\ \text{k}\Omega) \geq 10(3.9\ \text{k}\Omega)$$

$$210\ \text{k}\Omega \geq 39\ \text{k}\Omega\ (\textit{satisfied})$$

Eq. (4.32): $$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega}$$

$$= 2\ \text{V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\text{Eq. (4.34):} \quad V_E = V_B - V_{BE}$$
$$= 2\text{ V} - 0.7\text{ V}$$
$$= 1.3\text{ V}$$
$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.5\text{ k}\Omega} = \mathbf{0.867\text{ mA}}$$

compared to 0.85 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\text{ V} - (0.867\text{ mA})(10\text{ kV} + 1.5\text{ k}\Omega)$$
$$= 22\text{ V} - 9.97\text{ V}$$
$$= \mathbf{12.03\text{ V}}$$

versus 12.22 V obtained in Example 4.7.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer the approximate to the exact solution. Example 4.10 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.9

Repeat the exact analysis of Example 4.7 if β is reduced to 70, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution

This example is not a comparison of exact versus approximate methods but a testing of how much the *Q*-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{Th} = 3.55\text{ k}\Omega, \qquad E_{Th} = 2\text{ V}$$
$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (71)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 106.5\text{ k}\Omega}$$
$$= 11.81\ \mu\text{A}$$
$$I_{C_Q} = \beta I_B$$
$$= (70)(11.81\ \mu\text{A})$$
$$= 0.83\text{ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\text{ V} - (0.83\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= \mathbf{12.46\text{ V}}$$

Tabulating the results, we have:

β	I_{C_Q} (mA)	V_{CE_Q} (V)
140	0.85	12.22
70	0.83	12.46

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 140 to 70, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.

EXAMPLE 4.10

Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.33 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied but the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

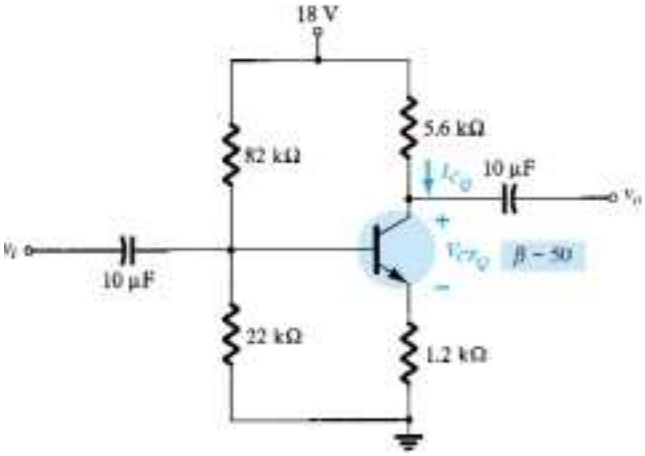


Figure 4.33 Voltage-divider configuration for Example 4.10.

Solution

Exact Analysis

$$\text{Eq. (4.33):} \quad \beta R_E \geq 10R_2$$

$$(50)(1.2\ \text{k}\Omega) \geq 10(22\ \text{k}\Omega)$$

$$60\ \text{k}\Omega \not\geq 220\ \text{k}\Omega\ (\textit{not satisfied})$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\ \text{k}\Omega \| 22\ \text{k}\Omega = 17.35\ \text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\ \text{k}\Omega(18\ \text{V})}{82\ \text{k}\Omega + 22\ \text{k}\Omega} = 3.81\ \text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\ \text{V} - 0.7\ \text{V}}{17.35\ \text{k}\Omega + (51)(1.2\ \text{k}\Omega)} = \frac{3.11\ \text{V}}{78.55\ \text{k}\Omega}$$

$$= 39.6\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(39.6\ \mu\text{A}) = \mathbf{1.98\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\ \text{V} - (1.98\ \text{mA})(5.6\ \text{k}\Omega + 1.2\ \text{k}\Omega)$$

$$= \mathbf{4.54\ V}$$

$$V_B = E_{\text{Th}} = 3.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 3.81\ \text{V} - 0.7\ \text{V} = 3.11\ \text{V}$$

$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11\ \text{V}}{1.2\ \text{k}\Omega} = \mathbf{2.59\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\ \text{V} - (2.59\ \text{mA})(5.6\ \text{k}\Omega + 1.2\ \text{k}\Omega)$$

$$= \mathbf{3.88\ V}$$

Tabulating the results, we have:

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, while V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to zero volts on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.24, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\ \text{V}} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0\ \text{mA}} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.34. Although the *Q*-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop with the results applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.35 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

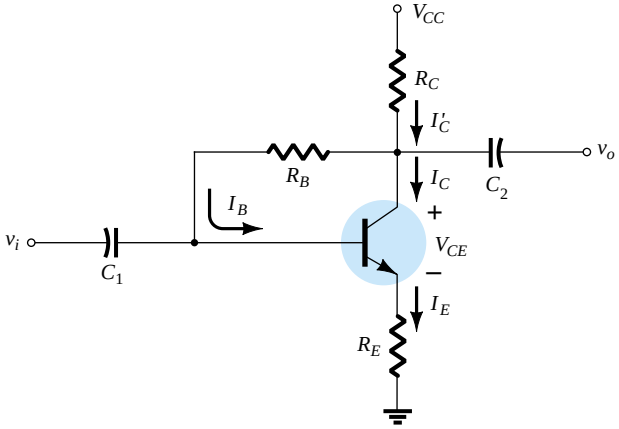


Figure 4.34 dc bias circuit with voltage feedback.

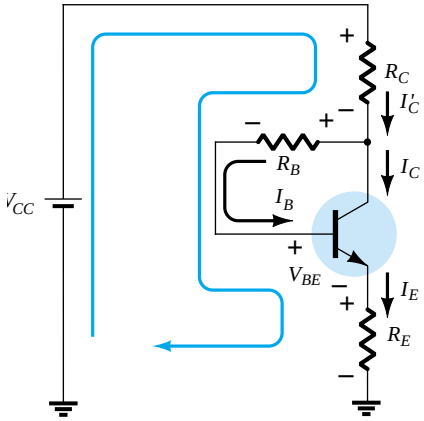


Figure 4.35 Base–emitter loop for the network of Fig. 4.34.

It is important to note that the current through R_C is not I_C but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ will result in

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \tag{4.41}$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, while the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has had the following format:

$$I_B = \frac{V'}{R_B + \beta R'}$$

with the absence of R' for the fixed-bias configuration, $R' = R_E$ for the emitter-bias setup (with $(\beta + 1) \cong \beta$), and $R' = R_C + R_E$ for the collector-feedback arrangement. The voltage V' is the difference between two voltage levels.

Since $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'}$$

In general, the larger $\beta R'$ is compared to R_B, the less the sensitivity of I_{C_Q} to variations in beta. Obviously, if $\beta R' \gg R_B$ and $R_B + \beta R' \cong \beta R'$, then

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'} \cong \frac{\beta V'}{\beta R'} = \frac{V'}{R'}$$

and I_{C_Q} is independent of the value of beta. Since R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is zero ohms for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

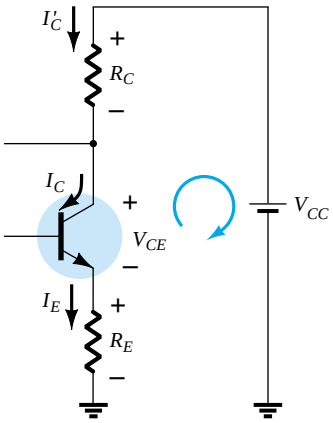


Figure 4.36 Collector–emitter loop for the network of Fig. 4.34.

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 4.34 is provided in Fig. 4.36. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \qquad (4.42)$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

EXAMPLE 4.11

Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.37.

Solution

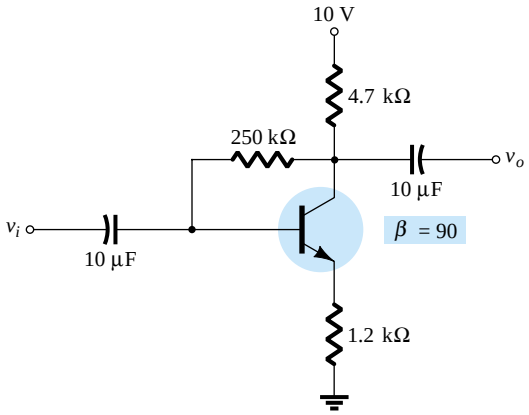


Figure 4.37 Network for Example 4.11.

Eq. (4.41): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\ V}$$

Repeat Example 4.11 using a beta of 135 (50% more than Example 4.11). *EXAMPLE 4.12*

Solution

It is important to note in the solution for I_B in Example 4.11 that the second term in the denominator of the equation is larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less the sensitivity to changes in beta. In this example the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (135)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 796.5\text{ k}\Omega} = \frac{9.3\text{ V}}{1046.5\text{ k}\Omega}$$

$$= 8.89\ \mu\text{A}$$

and

$$I_{C_Q} = \beta I_B$$

$$= (135)(8.89\ \mu\text{A})$$

$$= \mathbf{1.2\text{ mA}}$$

and

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.2\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 7.08\text{ V}$$

$$= \mathbf{2.92\text{ V}}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1% while the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q-point.

Determine the dc level of I_B and V_C for the network of Fig. 4.38. *EXAMPLE 4.13*

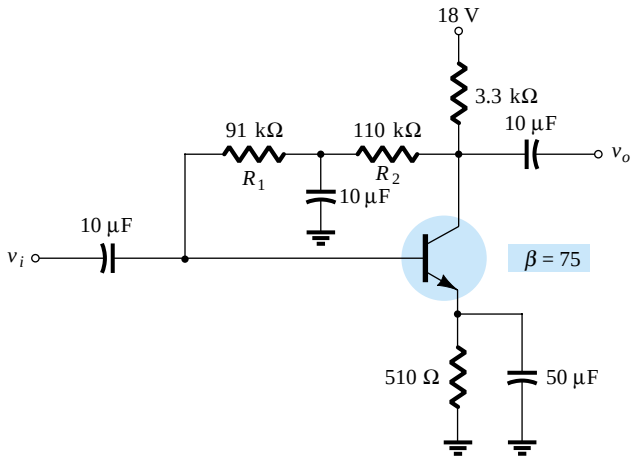


Figure 4.38 Network for Example 4.13.

Solution

In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence and $R_B = R_1 + R_2$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\text{ k}\Omega + 110\text{ k}\Omega) + (75)(3.3\text{ k}\Omega + 0.51\text{ k}\Omega)}$$

$$= \frac{17.3\text{ V}}{201\text{ k}\Omega + 285.75\text{ k}\Omega} = \frac{17.3\text{ V}}{486.75\text{ k}\Omega}$$

$$= \mathbf{35.5\ \mu A}$$

$$I_C = \beta I_B$$

$$= (75)(35.5\ \mu\text{A})$$

$$= 2.66\text{ mA}$$

$$V_C = V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C$$

$$= 18\text{ V} - (2.66\text{ mA})(3.3\text{ k}\Omega)$$

$$= 18\text{ V} - 8.78\text{ V}$$

$$= \mathbf{9.22\text{ V}}$$

Saturation Conditions

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} will be defined by the chosen bias configuration.

4.7 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a book of this type. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite di-

rectly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.34. The analysis is quite similar but does require dropping R_E from the applied equation.

EXAMPLE 4.14

For the network of Fig. 4.39:
(a) Determine I_{C_Q} and V_{CE_Q}.
(b) Find V_B, V_C, V_E, and V_{BC}.

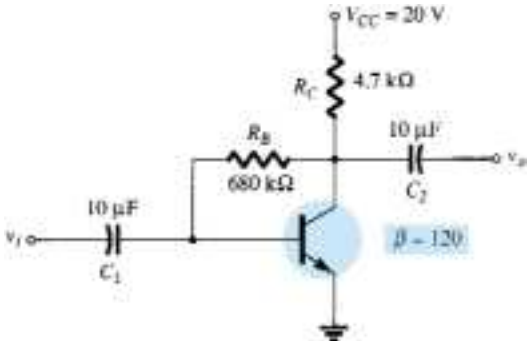


Figure 4.39 Collector feedback with $R_E = 0\ \Omega$.

Solution

(a) The absence of R_E reduces the reflection of resistive levels to simply that of R_C and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{680\text{ k}\Omega + (120)(4.7\text{ k}\Omega)} = \frac{19.3\text{ V}}{1.244\text{ M}\Omega}$$

$$= 15.51\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (120)(15.51\ \mu\text{A})$$

$$= \mathbf{1.86\text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (1.86\text{ mA})(4.7\text{ k}\Omega)$$

$$= \mathbf{11.26\text{ V}}$$

$$V_B = V_{BE} = \mathbf{0.7\text{ V}}$$

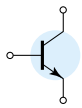
$$V_C = V_{CE} = \mathbf{11.26\text{ V}}$$

$$V_E = \mathbf{0\text{ V}}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 11.26\text{ V}$$

$$= \mathbf{-10.56\text{ V}}$$

In the next example, the applied voltage is connected to the emitter leg and R_C is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.



EXAMPLE 4.15 Determine V_C and V_B for the network of Fig. 4.40.

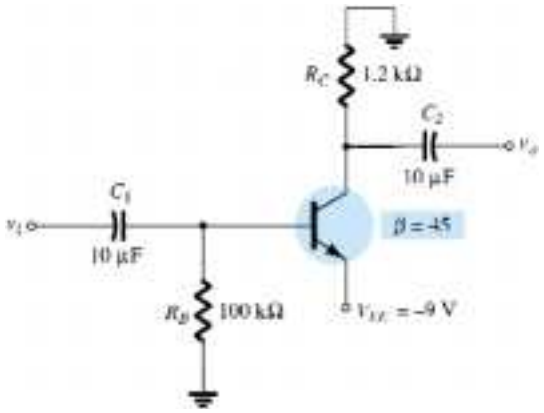


Figure 4.40 Example 4.15

Solution

Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop will result in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}$$

$$= \frac{8.3\text{ V}}{100\text{ k}\Omega}$$

$$= 83\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (45)(83\ \mu\text{A})$$

$$= 3.735\text{ mA}$$

$$V_C = -I_C R_C$$

$$= -(3.735\text{ mA})(1.2\text{ k}\Omega)$$

$$= \mathbf{-4.48\text{ V}}$$

$$V_B = -I_B R_B$$

$$= -(83\ \mu\text{A})(100\text{ k}\Omega)$$

$$= \mathbf{-8.3\text{ V}}$$

The next example employs a network referred to as an *emitter-follower* configuration. When the same network is analyzed on an ac basis, we will find that the output and input signals are in phase (one following the other) and the output voltage is slightly less than the applied signal. For the dc analysis the collector is grounded and the applied voltage is in the emitter leg.

Determine V_{CE_Q} and I_E for the network of Fig. 4.41.

EXAMPLE 4.16

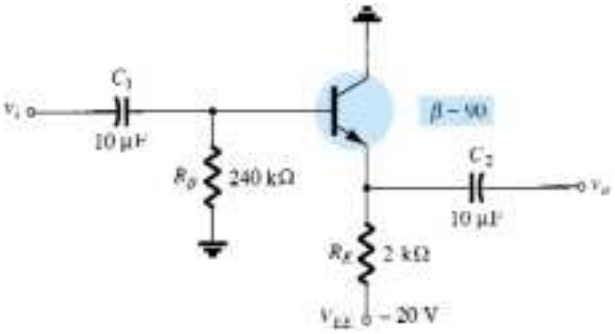


Figure 4.41 Common-collector (emitter-follower) configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

but
$$I_E = (\beta + 1) I_B$$

and
$$V_{EE} - V_{BE} - (\beta + 1) I_B R_E - I_B R_B = 0$$

with
$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Substituting values yields

$$I_B = \frac{20\ \text{V} - 0.7\ \text{V}}{240\ \text{k}\Omega + (91)(2\ \text{k}\Omega)}$$

$$= \frac{19.3\ \text{V}}{240\ \text{k}\Omega + 182\ \text{k}\Omega} = \frac{19.3\ \text{V}}{422\ \text{k}\Omega}$$

$$= 45.73\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (90)(45.73\ \mu\text{A})$$

$$= 4.12\ \text{mA}$$

Applying Kirchhoff's voltage law to the output circuit, we have

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

but
$$I_E = (\beta + 1) I_B$$

and
$$V_{CE_Q} = V_{EE} - (\beta + 1) I_B R_E$$

$$= 20\ \text{V} - (91)(45.73\ \mu\text{A})(2\ \text{k}\Omega)$$

$$= \mathbf{11.68\ V}$$

$$I_E = \mathbf{4.16\ mA}$$

All of the examples thus far have employed a common-emitter or common-collector configuration. In the next example we investigate the common-base configuration. In this situation the input circuit will be employed to determine I_E rather than I_B. The collector current is then available to perform an analysis of the output circuit.

EXAMPLE 4.17

Determine the voltage V_{CB} and the current I_B for the common-base configuration of Fig. 4.42.

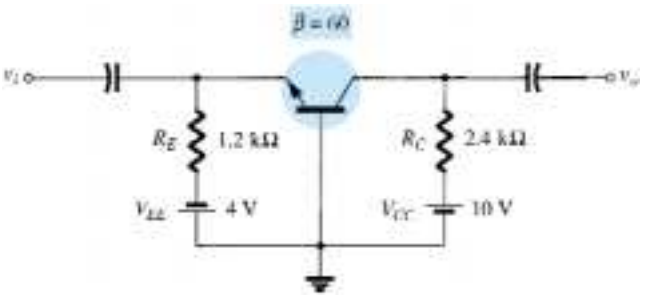


Figure 4.42 Common-base configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit yields

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

and

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Substituting values, we obtain

$$I_E = \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = 2.75\text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit gives

$$-V_{CB} + I_C R_C - V_{CC} = 0$$

and

$$V_{CB} = V_{CC} - I_C R_C \text{ with } I_C \cong I_E$$
$$= 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega)$$
$$= \mathbf{3.4\text{ V}}$$

$$I_B = \frac{I_C}{\beta}$$
$$= \frac{2.75\text{ mA}}{60}$$
$$= \mathbf{45.8\ \mu A}$$

Example 4.18 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

Determine V_C and V_B for the network of Fig. 4.43.

EXAMPLE 4.18

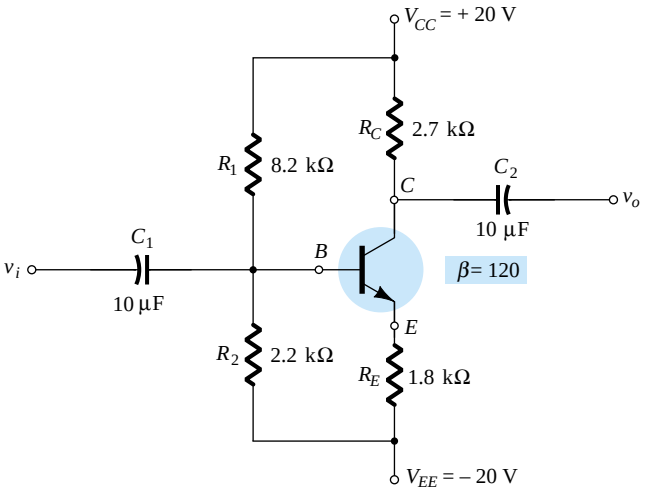


Figure 4.43 Example 4.18

Solution

The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.44 and 4.45.

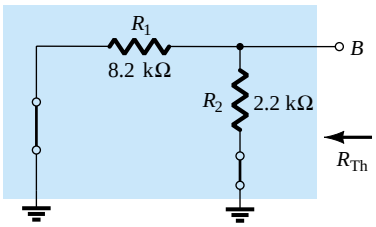


Figure 4.44 Determining R_{Th}.

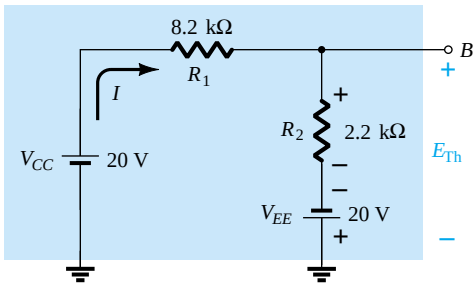


Figure 4.45 Determining E_{Th}.

R_{Th}:

$$R_{Th} = 8.2\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 1.73\ \text{k}\Omega$$

E_{Th}:

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\ \text{V} + 20\ \text{V}}{8.2\ \text{k}\Omega + 2.2\ \text{k}\Omega} = \frac{40\ \text{V}}{10.4\ \text{k}\Omega}$$

$$= 3.85\ \text{mA}$$

$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85\ \text{mA})(2.2\ \text{k}\Omega) - 20\ \text{V}$$

$$= -11.53\ \text{V}$$

The network can then be redrawn as shown in Fig. 4.46, where the application of Kirchhoff's voltage law will result in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$

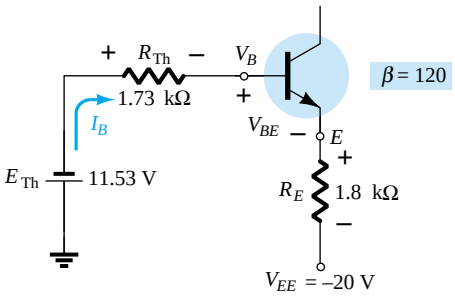


Figure 4.46 Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

and

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{20\text{ V} - 11.53\text{ V} - 0.7\text{ V}}{1.73\text{ k}\Omega + (121)(1.8\text{ k}\Omega)}$$

$$= \frac{7.77\text{ V}}{219.53\text{ k}\Omega}$$

$$= 35.39\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (120)(35.39\ \mu\text{A})$$

$$= 4.25\text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (4.25\text{ mA})(2.7\text{ k}\Omega)$$

$$= \mathbf{8.53\text{ V}}$$

$$V_B = -E_{Th} - I_B R_{Th}$$

$$= -(11.53\text{ V}) - (35.39\ \mu\text{A})(1.73\text{ k}\Omega)$$

$$= \mathbf{-11.59\text{ V}}$$

4.8 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{unk}} = \frac{V_R}{I_R} \tag{4.44}$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.44) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from specified levels. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.19

Given the device characteristics of Fig. 4.47a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.47b.

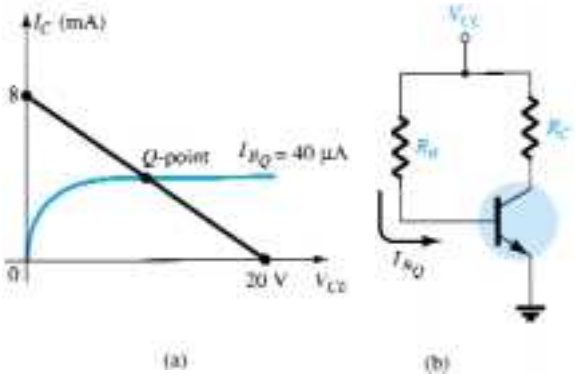


Figure 4.47 Example 4.19

Solution

From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE} = 0\ \text{V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\ \text{V} - 0.7\ \text{V}}{40\ \mu\text{A}} = \frac{19.3\,\text{V}}{40\ \mu\text{A}}$$

$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values:

$$R_C = 2.4\ \text{k}\Omega$$

$$R_B = 470\ \text{k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

EXAMPLE 4.20

Given that $I_{C_Q} = 2$ mA and $V_{CE_Q} = 10$ V, determine R_1 and R_C for the network of Fig. 4.48.

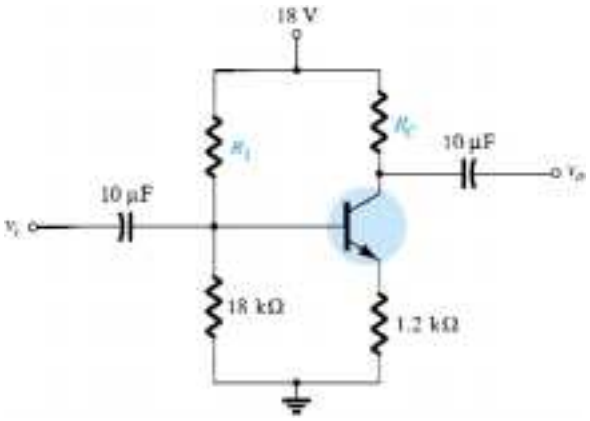


Figure 4.48 Example 4.20

Solution

$$V_E = I_E R_E \cong I_C R_E$$

$$= (2\ \text{mA})(1.2\ \text{k}\Omega) = 2.4\ \text{V}$$

$$V_B = V_{BE} + V_E = 0.7\ \text{V} + 2.4\ \text{V} = 3.1\ \text{V}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\ \text{V}$$

and

$$\frac{(18\ \text{k}\Omega)(18\ \text{V})}{R_1 + 18\ \text{k}\Omega} = 3.1\ \text{V}$$

$$324\ \text{k}\Omega = 3.1R_1 + 55.8\ \text{k}\Omega$$

$$3.1R_1 = 268.2\ \text{k}\Omega$$

$$R_1 = \frac{268.2\ \text{k}\Omega}{3.1} = \mathbf{86.52\ k\Omega}$$

Eq. (4.44):

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

with

$$V_C = V_{CE} + V_E = 10\ \text{V} + 2.4\ \text{V} = 12.4\ \text{V}$$

and

$$R_C = \frac{18\ \text{V} - 12.4\text{V}}{2\text{mA}}$$

$$= \mathbf{2.8\ k\Omega}$$

The nearest standard commercial values to R_1 are 82 and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 4.7 kΩ = 86.7 kΩ would result in a value very close to the design level.

EXAMPLE 4.21

The emitter-bias configuration of Fig. 4.49 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$, $I_{C_{sat}} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C, R_E, and R_B.

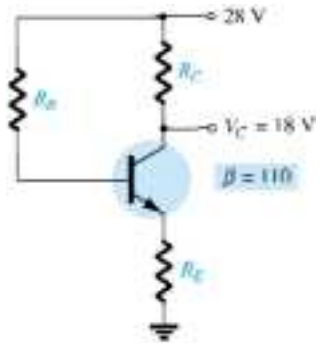


Figure 4.49 Example 4.21

Solution

$$I_{C_Q} = \tfrac{1}{2}I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ m}A} = \mathbf{2.5\ k\Omega}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

and

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= \mathbf{1\ k\Omega}$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36\ \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36\ \mu\text{A}} - 111 \text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

For standard values:

$$R_C = 2.4\ \text{k}\Omega$$
$$R_E = 1\ \text{k}\Omega$$
$$R_B = 620\ \text{k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we shall concentrate, however, on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.50. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

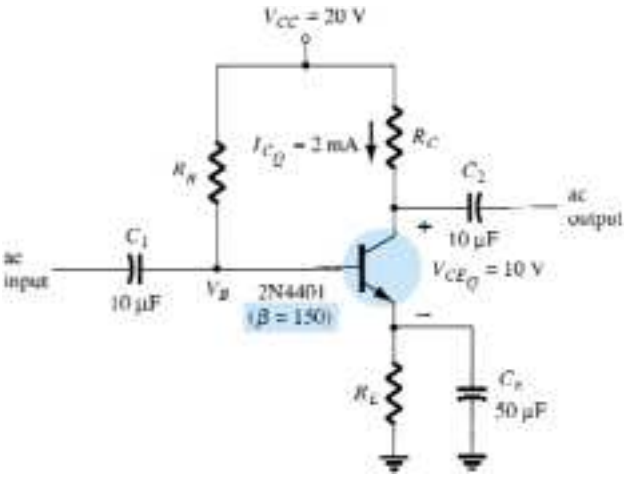


Figure 4.50 Emitter-stabilized bias circuit for design consideration.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector–emitter loop has two unknown quantities present—the resistors R_C and R_E. At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of voltage swing of the voltage from collector to emitter (to be noted when the ac re-

sponse is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.49 using the criteria just introduced for the emitter voltage.

EXAMPLE 4.22

Determine the resistor values for the network of Fig. 4.50 for the indicated operating point and supply voltage.

Solution

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\ k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\ k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$

$$\cong \mathbf{1.3\ M\Omega}$$

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.51 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage, V_E, as in the previous design consideration, leads to a direct straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

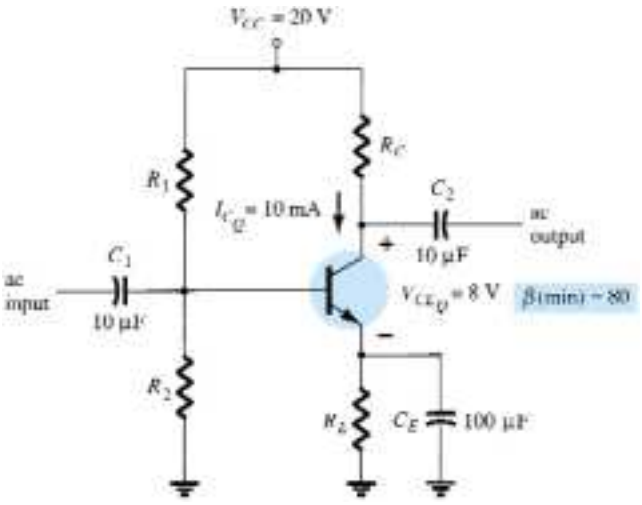
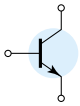


Figure 4.51 Current-gain-stabilized circuit for design considerations.



EXAMPLE 4.23

Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.51 for the operating point indicated.

Solution

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

The equations for the calculation of the base resistors R_1 and R_2 will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, R_1 and R_2. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through R_1 and R_2 should be approximately equal and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

Substitution yields

$$R_2 \leq \tfrac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

and

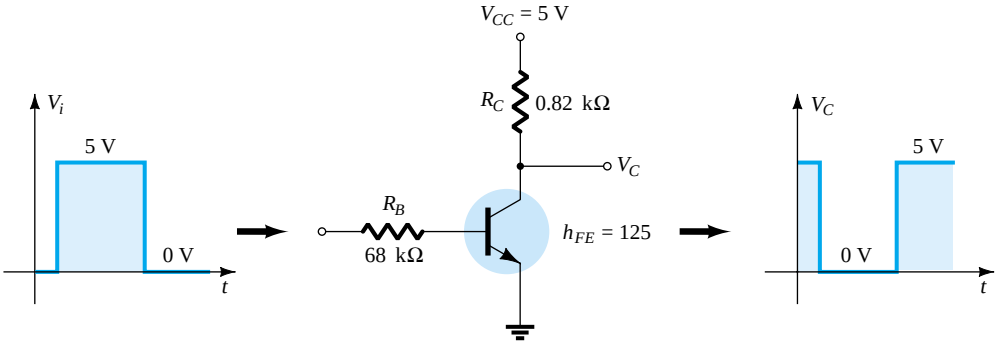
$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$

$$2.7R_1 = 27.68\text{ k}\Omega$$

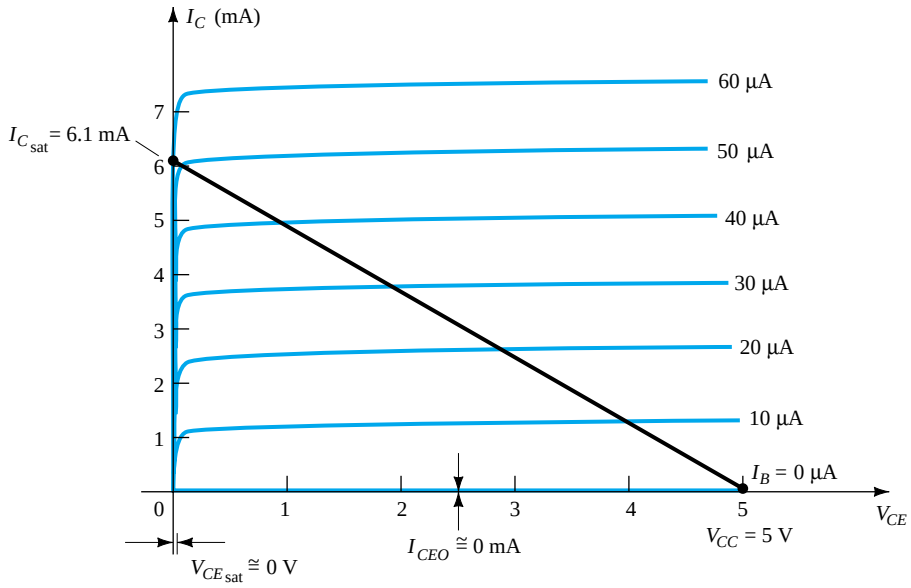
$$R_1 = \mathbf{10.25\ k\Omega} \quad \text{(use 10 k}\Omega\text{)}$$

4.9 TRANSISTOR SWITCHING NETWORKS

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control applications. The network of Fig. 4.52a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V.



(a)



(b)

Figure 4.52 Transistor inverter.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.52b. For our purposes we will assume that $I_C = I_{CEO} = 0$ mA when $I_B = 0$ μA (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.52b. In addition, we will assume that $V_{CE} = V_{CE_{sat}} = 0$ V rather than the typical 0.1- to 0.3-V level.

When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level. In Fig. 4.52b, this requires that $I_B > 50$ μA. The saturation level for the collector current for the circuit of Fig. 4.52a is defined by

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.45}$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$\boxed{I_B > \frac{I_{C_{sat}}}{\beta_{dc}}} \tag{4.46}$$

For the network of Fig. 4.52b, when $V_i = 5$ V, the resulting level of I_B is the following:

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (4.46) gives

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

which is satisfied. Certainly, any level of I_B greater than 60 μA will pass through a Q-point on the load line that is very close to the vertical axis.

For $V_i = 0$ V, $I_B = 0$ μA, and since we are assuming that $I_C = I_{CEO} = 0$ mA, the voltage drop across R_C as determined by $V_{R_C} = I_C R_C = 0$ V, resulting in $V_C = +5$ V for the response indicated in Fig. 4.52a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current I_C is quite high and the voltage V_{CE} very low. The result is a resistance level between the two terminals determined by

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

and depicted in Fig. 4.53.

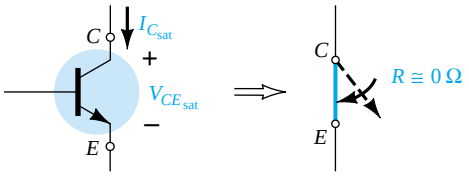


Figure 4.53 Saturation conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{sat}}$ such as 0.15 V gives

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\ \Omega$$

which is a relatively low value and $\cong 0\ \Omega$ when placed in series with resistors in the kilohm range.

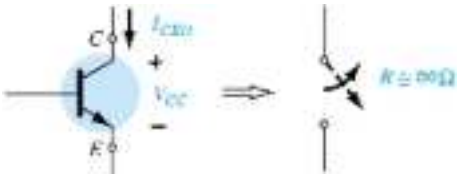


Figure 4.54 Cutoff conditions and the resulting terminal resistance.

For $V_i = 0$ V, as shown in Fig. 4.54, the cutoff condition will result in a resistance level of the following magnitude:

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \infty\ \boldsymbol{\Omega}$$

resulting in the open-circuit equivalence. For a typical value of $I_{CEO} = 10\ \mu$A, the magnitude of the cutoff resistance is

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\ \mu\text{A}} = \mathbf{500\ k\Omega}$$

which certainly approaches an open-circuit equivalence for many situations.

EXAMPLE 4.24

Determine R_B and R_C for the transistor inverter of Fig. 4.55 if $I_{C_{\text{sat}}} = 10$ mA.

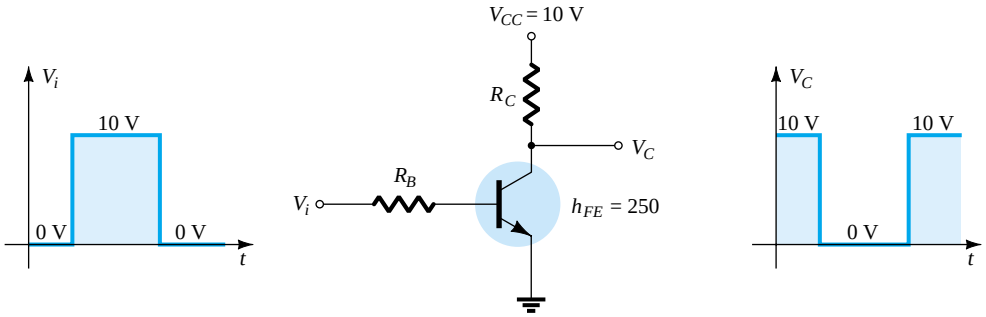


Figure 4.55 Inverter for Example 4.24.

Solution

At saturation:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation:

$$I_B \cong \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{10\text{ mA}}{250} = 40\ \mu\text{A}$$

Choosing $I_B = 60\ \mu$A to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain $$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\ \mu\text{A}} = 155\ \text{k}\Omega$$

Choose $R_B = 150\ \text{k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\ \text{k}\Omega} = 62\ \mu\text{A}$$

and $$I_B = 62\ \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = 40\ \mu\text{A}$$

Therefore, use $R_B = \mathbf{150\ k\Omega}$ and $R_C = \mathbf{1\ k\Omega}$**.**

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.56. The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and defined by

$$t_{\text{on}} = t_r + t_d \tag{4.47}$$

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.

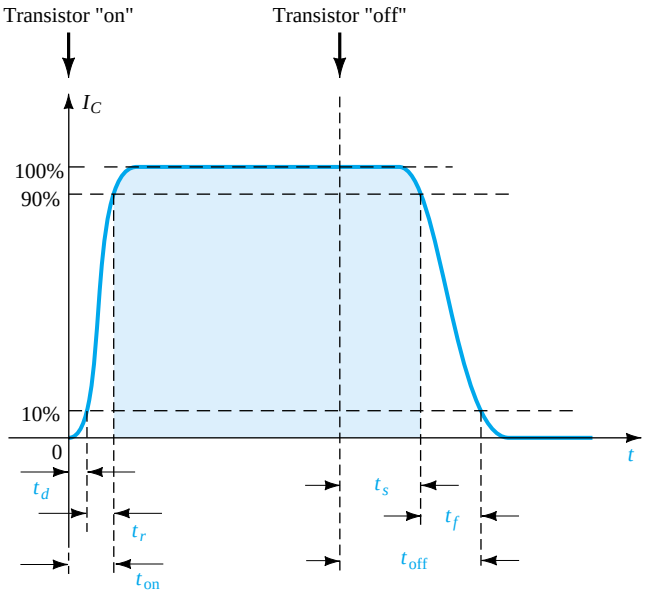


Figure 4.56 Defining the time intervals of a pulse waveform.

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$t_{\text{off}} = t_s + t_f \tag{4.48}$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at $I_C = 10$ mA, we find that

$$t_s = 120 \text{ ns}$$

$$t_d = 25 \text{ ns}$$

$$t_r = 13 \text{ ns}$$

and $$t_f = 12 \text{ ns}$$

so that $$t_{on} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = \mathbf{38 \text{ ns}}$$

and $$t_{off} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = \mathbf{132 \text{ ns}}$$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises.

$$t_{on} = \mathbf{12 \text{ ns}} \quad \text{and} \quad t_{off} = \mathbf{18 \text{ ns}}$$

4.10 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

For an "on" transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.

The proper connections for measuring V_{BE} appear in Fig. 4.57. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V, or negative in value would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used but a negative reading should be expected.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of V_{CE} in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless being employed in a switching mode. However:

For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

For $V_{CC} = 20$ V, a reading of V_{CE} of 1 to 2 V or 18 to 20 V as measured in Fig. 4.58 is certainly an uncommon result, and unless knowingly designed for this response the design and operation should be investigated. If $V_{CE} = 20$ V (with $V_{CC} = 20$ V) at least two possibilities exist—either the device (BJT) is damaged and has the

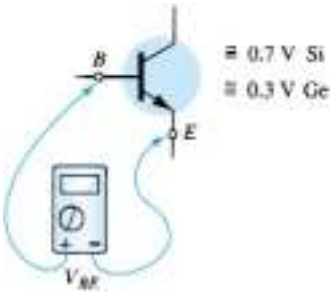


Figure 4.57 Checking the dc level of V_{BE}.

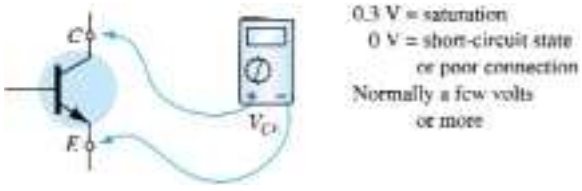


Figure 4.58 Checking the dc level of V_{CE}.

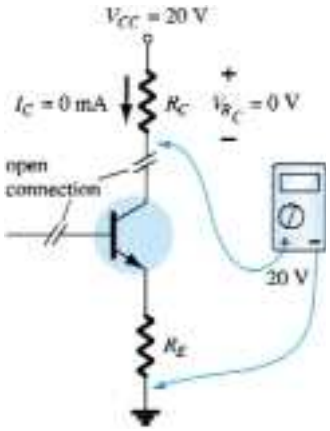


Figure 4.59 Effect of a poor connection or damaged device.

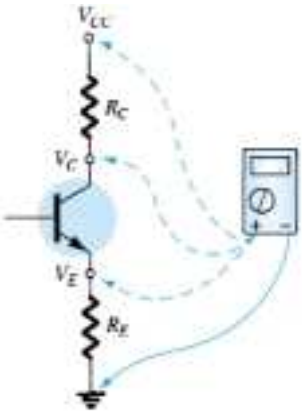


Figure 4.60 Checking voltage levels with respect to ground.

characteristics of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.59, establishing I_C at 0 mA and $V_{R_C} = 0$ V. In Fig. 4.59, the black lead of the voltmeter is connected to the common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a resulting drop across R_C will result in a reading of 20 V. If the meter is connected to the collector terminal of the BJT, the reading will be 0 V since V_{CC} is blocked from the active device by the open circuit. One of the most common errors in the laboratory experience is the use of the wrong resistance value for a given design. Imagine the impact of using a 680-Ω resistor for R_B rather than the design value of 680 kΩ. For $V_{CC} = 20$ V and a fixed-bias configuration, the resulting base current would be

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\ \Omega} = 28.4\text{ mA}$$

rather than the desired 28.4 μA—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Since actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is actual values closer to theoretical levels and some insurance that the correct resistance value is being employed.

There are times when frustration will develop. You have checked the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection between the wire and the end connection of a lead is faulty? How often has simply touching a lead at the proper point created a "make or break" situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and "touching" the important terminals with the red (positive) lead. In Fig. 4.60, if the red lead is connected directly to V_{CC}, it should read V_{CC} volts since the network has one common ground for the supply and network parameters. At V_C the reading should be less, as determined by the drop across R_C and V_E should be less than V_C by the collector–emitter voltage V_{CE}. The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If V_{R_C} and V_{R_E} are reasonable values but V_{CE} is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if V_{CE} registers a level of about 0.3 V as defined by $V_{CE} = V_C - V_E$ (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than "breaking" the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.

EXAMPLE 4.25

Based on the readings provided in Fig. 4.61, determine whether the network is operating properly and, if not, the probable cause.

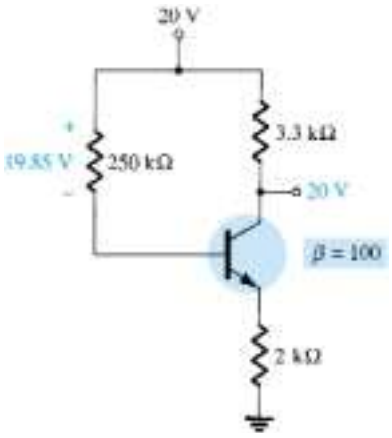


Figure 4.61 Network for Example 4.25.

Solution

The 20 V at the collector immediately reveals that $I_C = 0$ mA, due to an open circuit or a nonoperating transistor. The level of $V_{R_B} = 19.85$ V also reveals that the transistor is "off" since the difference of $V_{CC} - V_{R_B} = 0.15$ V is less than that required to turn "on" the transistor and provide some voltage for V_E. In fact, if we assume a short circuit condition from base to emitter, we obtain the following current through R_B:

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20\text{ V}}{252\text{ k}\Omega} = 79.4\ \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85\text{ V}}{250\text{ k}\Omega} = 79.4\ \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (101)(2\text{ k}\Omega)} = \frac{19.3\text{ V}}{452\text{ k}\Omega} = 42.7\ \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

EXAMPLE 4.26

Based on the readings appearing in Fig. 4.62, determine whether the transistor is "on" and the network is operating properly.

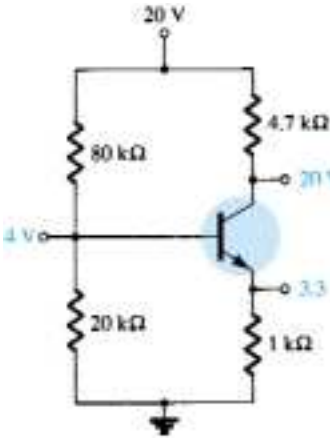


Figure 4.62 Network for Example 4.26.

Solution

Based on the resistor values of R_1 and R_2 and the magnitude of V_{CC}, the voltage $V_B = 4$ V seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an "on" transistor. However, the 20 V at the collector reveals that $I_C = 0$ mA, although the connection to the supply must be "solid" or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between R_C and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohmmeter, and if okay, the transistor should be checked using one of the methods described in Chapter 3.

4.11 *PNP* TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of I_B is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

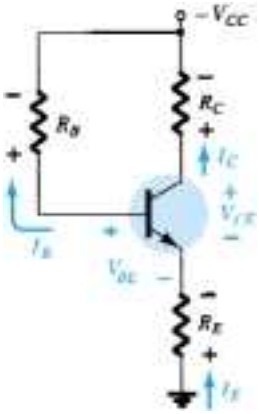


Figure 4.63 *pnp* transistor in an emitter-stabilized configuration.

As noted in Fig. 4.63, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.63, both V_{BE} and V_{CE} will be negative quantities.

Applying Kirchhoff's voltage law to the base–emitter loop will result in the following equation for the network of Fig. 4.63:

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.49}$$

The resulting equation is the same as Eq. (4.17) except for the sign for V_{BE}. However, in this case $V_{BE} = -0.7$ V and the substitution of values will result in the same sign for each term of Eq. (4.49) as Eq. (4.17). Keep in mind that the direction of I_B is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.63.

For V_{CE} Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ gives

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \tag{4.50}$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Since V_{CC} will be larger than the magnitude of the succeeding term, the voltage V_{CE} will have a negative sign, as noted in an earlier paragraph.

Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.64. *EXAMPLE 4.27*

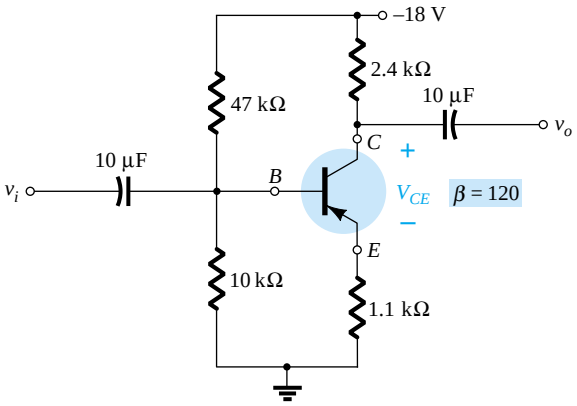


Figure 4.64 *pnp* transistor in a voltage-divider bias configuration.

Solution

Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$(120)(1.1\ \text{k}\Omega) \geq 10(10\ \text{k}\Omega)$$

$$132\ \text{k}\Omega \geq 100\ \text{k}\Omega\ (\textit{satisfied})$$

Solving for V_B, we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10\ \text{k}\Omega)(-18\ \text{V})}{47\ \text{k}\Omega + 10\ \text{k}\Omega} = -3.16\ \text{V}$$

Note the similarity in format of the equation with the resulting negative voltage for V_B.

Applying Kirchhoff's voltage law around the base–emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$V_E = -3.16\ \text{V} - (-0.7\ \text{V})$$
$$= -3.16\ \text{V} + 0.7\ \text{V}$$
$$= -2.46\ \text{V}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation $V_E = V_B - V_{BE}$ would be exactly the same. The only difference surfaces when the values are substituted.

The current

$$I_E = \frac{V_E}{R_E} = \frac{2.46\ \text{V}}{1.1\ \text{k}\Omega} = 2.24\ \text{mA}$$

For the collector–emitter loop:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

$$V_{CE} = -18\text{ V} + (2.24\text{ mA})(2.4\text{ k}\Omega + 1.1\text{ k}\Omega)$$
$$= -18\text{ V} + 7.84\text{ V}$$
$$= \mathbf{-10.16\text{ V}}$$

4.12 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 7.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.1 reveals how the level of I_{CO} and V_{BE} changed with increase in temperature for a particular transistor. At room temperature (about 25°C) I_{CO} = 0.1 nA, while at 100°C (boiling point of water) I_{CO} is about 200 times larger at 20 nA. For the same temperature variation, β increased from 50 to 80 and V_{BE} dropped from 0.65 to 0.48 V. Recall that I_B is quite sensitive to the level of V_{BE}, especially for levels beyond the threshold value.

TABLE 4.1 Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE}(V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

The effect of changes in leakage current (I_{CO}) and current gain (β) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.65a and b. Figure 4.65 shows how the transistor collector characteristics change from a temperature of 25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise but also an increase in beta, as revealed by the larger spacing between curves.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.65a at $I_B = 30\ \mu$A. Since the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.65b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector–emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not

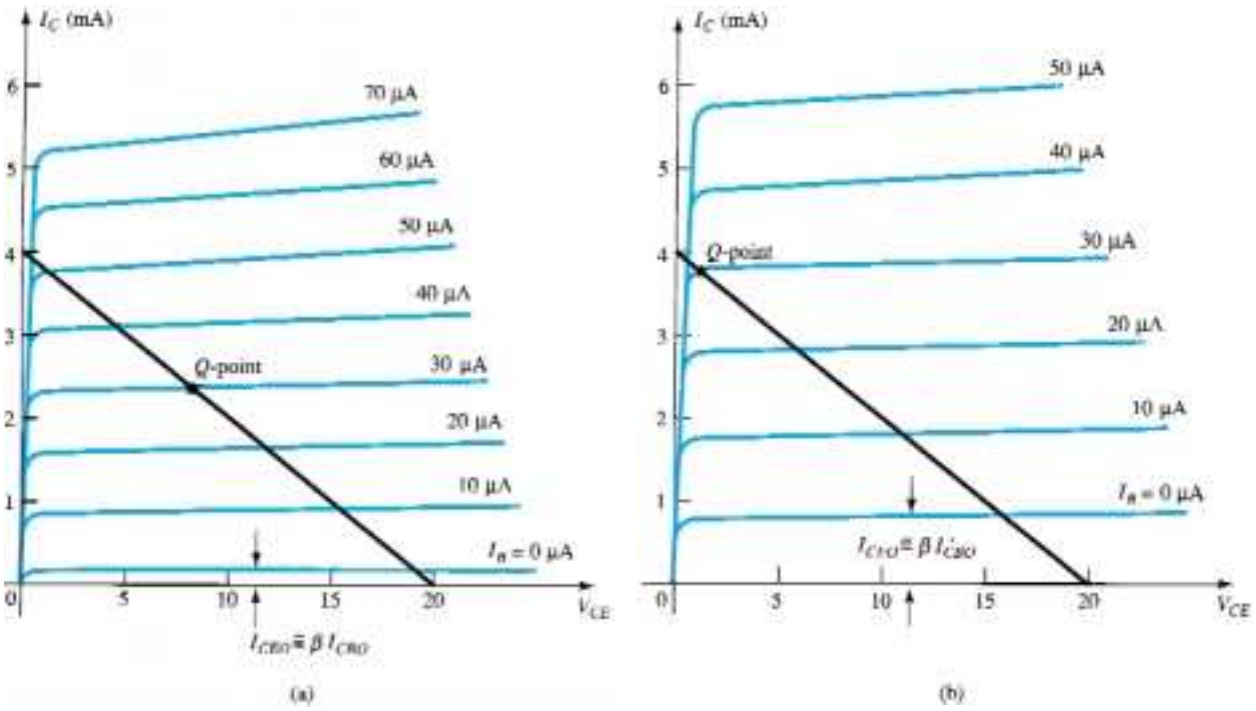


Figure 4.65 Shift in dc bias point (*Q*-point) due to change in temperature: (a) 25°C; (b) 100°C.

be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor, *S*, is defined for each of the parameters affecting bias stability as listed below:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \tag{4.51}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \tag{4.52}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \tag{4.53}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.51–4.53) to be sensitivity factors because:

The higher the stability factor, the more sensitive the network to variations in that parameter.

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject.

$S(I_{CO})$: EMITTER-BIAS CONFIGURATION

For the emitter-bias configuration, an analysis of the network will result in

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E} \tag{4.54}$$

For $R_B/R_E \gg (\beta + 1)$, Eq. (4.54) will reduce to the following:

$$S(I_{CO}) = \beta + 1 \tag{4.55}$$

as shown on the graph of $S(I_{CO})$ versus R_B/R_E in Fig. 4.66.

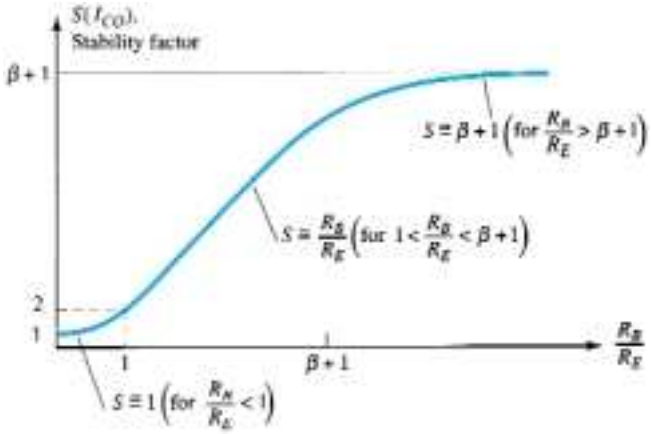


Figure 4.66 Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the emitter-bias configuration.

For $R_B/R_E \ll 1$, Eq. (4.54) will approach the following level (as shown in Fig. 4.66):

$$S(I_{CO}) = (\beta + 1)\frac{1}{(\beta + 1)} = \rightarrow 1 \tag{4.56}$$

revealing that the stability factor will approach its lowest level as R_E becomes sufficiently large. Keep in mind, however, that good bias control normally requires that R_B be greater than R_E. The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.66 that the lowest value of $S(I_{CO})$ is 1, revealing that I_C will always increase at a rate equal to or greater than I_{CO}.

For the range where R_B/R_E ranges between 1 and $(\beta + 1)$, the stability factor will be determined by

$$S(I_{CO}) \cong \frac{R_B}{R_E} \tag{4.57}$$

as shown in Fig. 4.66. The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches $(\beta + 1)$.

EXAMPLE 4.28

Calculate the stability factor and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following emitter-bias arrangements.
(a) $R_B/R_E = 250$ $(R_B = 250R_E)$
(b) $R_B/R_E = 10$ $(R_B = 10R_E)$.
(c) $R_B/R_E = 0.01$ $(R_E = 100R_B)$.

Solution

(a) $$S(I_{CO}) = (\beta + 1)\,1 + \frac{R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 250}{51 + 250}\right) = 51\left(\frac{251}{301}\right)$$
$$\cong \mathbf{42.53}$$
which begins to approach the level defined by $\beta + 1 = 51$.

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (42.53)(19.9\text{ nA})$$
$$\cong \mathbf{0.85\ \mu A}$$

(b) $$S(I_{CO}) = (\beta + 1)\,\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 10}{51 + 10}\right) = 51\left(\frac{11}{61}\right)$$
$$\cong \mathbf{9.2}$$
$$\Delta I_C = [S(I_{CO})](\Delta\, I_{CO}) = (9.2)(19.9\text{ nA})$$
$$\cong \mathbf{0.18\ \mu A}$$

(c) $$S(I_{CO}) = (\beta + 1)\,\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 0.01}{51 + 0.01}\right) = 51\left(\frac{1.01}{51.01}\right)$$
$$\cong \mathbf{1.01}$$

which is certainly very close to the level of 1 forecast if $R_B/R_E \ll 1$.

$$\Delta I_C = [S(I_{CO})](\Delta\, I_{CO}) = 1.01(19.9\text{ nA})$$
$$= \mathbf{20.1\ nA}$$

Example 4.28 reveals how lower and lower levels of I_{CO} for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in I_C is considerably different in a circuit having ideal stability $(S = 1)$ from one having a stability factor of 42.53, the change in I_C is not that significant. For example, the amount of change in I_C from a dc bias current set at, say, 2 mA, would be from 2 to 2.085 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of I_{CO} have had a very positive impact on the stability question.

FIXED-BIAS CONFIGURATION

For the fixed-bias configuration, if we multiply the top and bottom of Eq. (4.54) by R_E and then plug in $R_E = 0\ \Omega$, the following equation will result:

$$\boxed{S(I_{CO}) = \beta + 1} \tag{4.58}$$

Note that the resulting equation matches the maximum value for the emitter-bias configuration. The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.

Voltage-Divider Bias Configuration

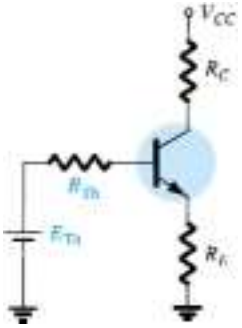


Figure 4.67 Equivalent circuit for the voltage-divider configuration.

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.67, for the voltage-divider bias configuration. For the network of Fig. 4.67, the equation for $S(I_{CO})$ is the following:

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_{Th}/R_E}{(\beta + 1) + R_{Th}/R_E} \tag{4.59}$$

Note the similarities with Eq. (4.54), where it was determined that $S(I_{CO})$ had its lowest level and the network had its greatest stability when $R_E > R_B$. For Eq. (4.59), the corresponding condition is $R_E > R_{Th}$ or R_{Th}/R_E should be as small as possible. For the voltage-divider bias configuration, R_{Th} can be much less than the corresponding R_B of the emitter-bias configuration and still have an effective design.

Feedback-Bias Configuration (R_E 5 0 Ω)

In this case,

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \tag{4.60}$$

Since the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.68a, the equation for the base current is the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$I_C = \beta I_B + (\beta + 1)I_{CO} \tag{4.61}$$

If I_C as defined by Eq. (4.61) should increase due to an increase in I_{CO}, there is nothing in the equation for I_B that would attempt to offset this undesirable increase in current level (assuming V_{BE} remains constant). In other words, the level of I_C would continue to rise with temperature, with I_B maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.68b, however, an increase in I_C due to an increase in I_{CO} will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of I_B as determined by the following equation:

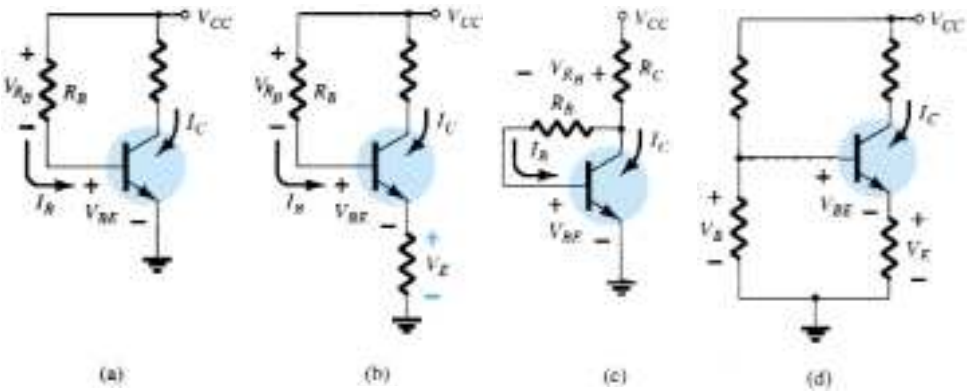


Figure 4.68 Review of biasing managements and the stability factor $S(I_{CO})$.

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B} \tag{4.62}$$

A drop in I_B will have the effect of reducing the level of I_C through transistor action and thereby offset the tendency of I_C to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.68c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If I_C should increase due to an increase in temperature, the level of V_{R_C} will increase in the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C} \uparrow}{R_B} \tag{4.63}$$

and the level of I_B will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant I_C begins to rise the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.68d. If the condition $\beta R_E \geqslant 10R_2$ is satisfied, the voltage V_B will remain fairly constant for changing levels of I_C. The base-to-emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If I_C should increase, V_E will increase as described above, and for a constant V_B the voltage V_{BE} will drop. A drop in V_{BE} will establish a lower level of I_B, which will try to offset the increased level of I_C.

$S(V_{BE})$

The stability factor defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

will result in the following equation for the emitter-bias configuration:

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} \tag{4.64}$$

Substituting $R_E = 0\ \Omega$ as occurs for the fixed-bias configuration will result in

$$S(V_{BE}) = -\frac{\beta}{R_B} \tag{4.65}$$

Equation (4.64) can be written in the following form:

$$S(V_{BE}) = \frac{-\beta/R_E}{R_B/R_E + (\beta + 1)} \tag{4.66}$$

Substituting the condition $(\beta + 1) \gg R_B/R_E$ will result in the following equation for $S(V_{BE})$:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + 1} \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E}} \tag{4.67}$$

revealing that the larger the resistance R_E, the lower the stability factor and the more stable the system.

EXAMPLE 4.29

Determine the stability factor $S(V_{BE})$ and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following bias arrangements.
(a) Fixed-bias with $R_B = 240\ \text{k}\Omega$ and $\beta = 100$.
(b) Emitter-bias with $R_B = 240\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, and $\beta = 100$.
(c) Emitter-bias with $R_B = 47\ \text{k}\Omega$, $R_E = 4.7\ \text{k}\Omega$, and $\beta = 100$.

Solution

(a) Eq. (4.65): $S(V_{BE}) = -\dfrac{\beta}{R_B}$

$$= -\frac{100}{240\ \text{k}\Omega}$$

$$= \mathbf{-0.417 \times 10^{-3}}$$

and $\Delta I_C = [S(V_{BE})](\Delta V_{BE})$

$$= (-0.417 \times 10^{-3})(0.48\ \text{V} - 0.65\ \text{V})$$

$$= (-0.417 \times 10^{-3})(-0.17\ \text{V})$$

$$= \mathbf{70.9\ \mu A}$$

(b) In this case, $(\beta + 1) = 101$ and $R_B/R_E = 240$. The condition $(\beta + 1) \gg R_B/R_E$ is not satisfied, negating the use of Eq. (4.67) and requiring the use of Eq. (4.64).

Eq. (4.64): $S(V_{BE}) = \dfrac{-\beta}{R_B + (\beta + 1)R_E}$

$$= \frac{-100}{240\ \text{k}\Omega + (101)1\ \text{k}\Omega} = -\frac{100}{341\ \text{k}\Omega}$$

$$= \mathbf{-0.293 \times 10^{-3}}$$

which is about 30% less than the fixed-bias value due to the additional $(\beta + 1)R_E$ term in the denominator of the $S(V_{BE})$ equation.

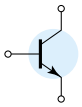
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$

$$= (-0.293 \times 10^{-3})(-0.17\ V)$$

$$\cong \mathbf{50\ \mu A}$$

(c) In this case,

$$(\beta + 1) = 101 \gg \frac{R_B}{R_E} = \frac{47\ \text{k}\Omega}{4.7\ \text{k}\Omega} = 10\ (\textit{satisfied})$$



Eq. (4.67): $$S(V_{BE}) = -\frac{1}{R_E}$$

$$= -\frac{1}{4.7\ \text{k}\Omega}$$

$$= \mathbf{-0.212 \times 10^{-3}}$$

and $$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$

$$= (-0.212 \times 10^{-3})(-0.17\ \text{V})$$

$$= \mathbf{36.04\ \mu A}$$

In Example 4.29, the increase of 70.9 μA will have some impact on the level of I_{C_Q}. For a situation where $I_{C_Q} = 2$ mA, the resulting collector current will increase to

$$I_{C_Q} = 2\ \text{mA} + 70.9\ \mu\text{A}$$

$$= 2.0709\ \text{mA}$$

a 3.5% increase.

For the voltage-divider configuration, the level of R_B will be changed to R_{Th} in Eq. (4.64) (as defined by Fig. 4.67). In Example 4.29, the use of $R_B = 47$ kΩ is a questionable design. However, R_{Th} for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for $S(V_{BE})$ for the feedback network will be similar to that of Eq. (4.64) with R_E replaced by R_C.

S(β)

The last stability factor to be investigated is that of $S(\beta)$. The mathematical development is more complex than that encountered for $S(I_{CO})$ and $S(V_{BE})$, as suggested by the following equation for the emitter-bias configuration:

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)} \tag{4.68}$$

The notation I_{C1} and β_1 is used to define their values under one set of network conditions, while the notation β_2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

EXAMPLE 4.30

Determine I_{C_Q} at a temperature of 100°C if $I_{C_Q} = 2$ mA at 25°C. Use the transistor described by Table 4.1, where $\beta_1 = 50$ and $\beta_2 = 80$, and a resistance ratio R_B/R_E of 20.

Solution

Eq. (4.68): $$S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

$$= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050}$$

$$= \mathbf{8.32 \times 10^{-6}}$$

and $$\Delta I_C = [S(\beta)][\Delta\beta]$$

$$= (8.32 \times 10^{-6})(30)$$

$$\cong \mathbf{0.25\ mA}$$

In conclusion therefore the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

The fixed-bias configuration is defined by $S(\beta) = I_{C_1}/\beta_1$ and R_B of Eq. (4.68) can be replaced by R_{Th} for the voltage-divider configuration.

For the collector feedback configuration with $R_E = 0\ \Omega$,

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + R_C(1 + \beta_2))} \tag{4.69}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation:

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \tag{4.70}$$

The equation may initially appear quite complex, but take note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in I_C from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.70) becomes the following:

$$\Delta I_C = (\beta + 1)\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta \tag{4.71}$$

after substituting the stability factors as derived in this section. Let us now use Table 4.1 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\Delta I_{CO} = 20\ \text{nA} - 0.1\ \text{nA} = 19.9\ \text{nA}$$

$$\Delta V_{BE} = 0.48\ \text{V} - 0.65\ \text{V} = -0.17\ \text{V} \quad \text{(note the sign)}$$

and

$$\Delta\beta = 80 - 50 = 30$$

Starting with a collector current of 2 mA with an R_B of 240 kΩ, the resulting change in I_C due to an increase in temperature of 75°C is the following:

$$\Delta I_C = (50 + 1)(19.9\ \text{nA}) - \frac{50}{240\ \text{k}\Omega}(-0.17\ \text{V}) + \frac{2\ \text{mA}}{50}(30)$$

$$= 1.01\ \mu\text{A} + 35.42\ \mu\text{A} + 1200\ \mu\text{A}$$

$$= 1.236\ \text{mA}$$

which is a significant change due primarily to the change in β. The collector current has increased from 2 to 3.236 mA—but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration were employed with a ratio $R_{\text{Th}}/R_E = 2$ and $R_E = 4.7\ k\Omega$, then

$$S(I_{CO}) = 2.89, \qquad S(V_{BE}) = -0.2 \times 10^{-3}, \qquad S(\beta) = 1.445 \times 10^{-6}$$

and

$$\Delta I_C = (2.89)(19.9\ \text{nA}) - 0.2 \times 10^{-3}(-0.17\ \text{V}) + 1.445 \times 10^{-6}(30)$$

$$= 57.51\ \text{nA} + 34\ \mu\text{A} + 43.4\ \mu\text{A}$$

$$= 0.077\ \text{mA}$$

The resulting collector current is 2.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case, $S(\beta)$ did not override the other two factors and the effects of $S(V_{BE})$ and $S(I_{CO})$ were equally important. In fact, at higher temperatures, the effects of $S(I_{CO})$ and $S(V_{BE})$ will be greater than $S(\beta)$ for the device of Table 4.1. For temperatures below 25°C, I_C will decrease with increasingly negative temperature levels.

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques that continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

4.13 PSPICE WINDOWS

Voltage-Divider Configuration

The results of Example 4.7 will now be verified using PSpice Windows. Using methods described in previous chapters, the network of Fig. 4.69 can be constructed. Recall that the transistor can be found in the **EVAL.slb** library, the dc source under **SOURCE.slb,** and the resistor under **ANALOG.slb.** The capacitor will also appear in the **ANALOG.slb** library. Three **VIEWPOINTS** appear in Fig. 4.69 as obtained from the **SPECIAL.slb** library. The collector current will be sensed by the **IPROBE** option, also appearing in the **SPECIAL.slb** library. Recall that a positive result is obtained for **IPROBE** if the direction of conventional current enters that side of the symbol with the internal curve representing the scale of the meter. We will want to set the value of beta for the transistor to match that of the example. This is accom-

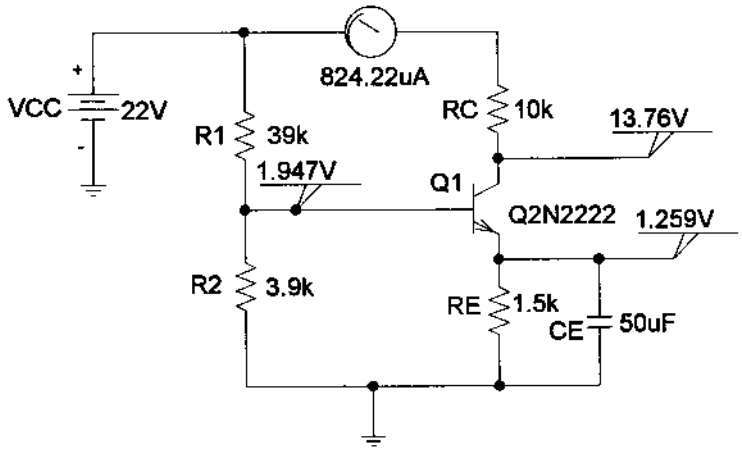


Figure 4.69 Applying PSpice Windows to the voltage-divider configuration of Example 4.7.

plished by clicking on the transistor symbol (to obtain the red outline) followed by **Edit-Model-Edit Instance Model (text)** to obtain the **Model Editor.** Then **Bf** is changed to 140 to match the value of Example 4.7. Click **OK,** and the network is set up for the analysis.

In this case, since we are only interested in the dc response, the **Probe Setup** under **Analysis** should enable **Do not auto-run Probe.** It will save us from having to deal with the Probe response before viewing the output file or screen. The sequence **Analysis-Simulate** will result in the dc levels appearing in Fig. 4.69, which closely match those of Example 4.7. The collector-to-emitter voltage is 13.76 V − 1.259 V = 12.5 V, versus 12.22 V of Example 4.7, and the collector current is 0.824 mA, versus 0.85 mA. Any differences are due to the fact that we are using an actual transistor with a host of parameters not considered in our analysis. Recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

Since the voltage-divider network is one that is to have a low sensitivity to changes in beta, let us return to the transistor and replace the beta of 140 with the default value of 225.9 and examine the results. The analysis will result in the dc levels appearing in Fig. 4.70, which are very close to those of Fig. 4.69.

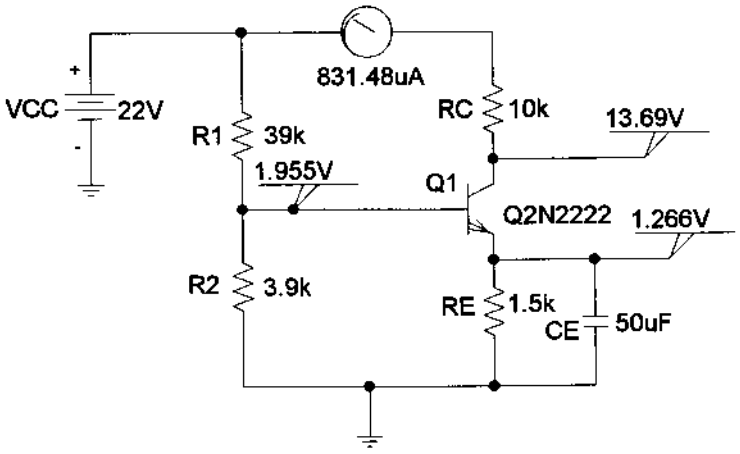


Figure 4.70 Response obtained after changing β from 140 to 255.9 for the network of Figure 4.69.

The collector-to-emitter voltage is 13.69 V − 1.266 V = 12.42 V, which is very close to that obtained with a much lower beta. The collector current is actually closer to the hand-calculated level, 0.832 mA versus 0.85 mA. There is no question, therefore, that the voltage-divider configuration demonstrates a low sensitivity to changes in beta. Recall, however, that the fixed-bias configuration was very sensitive to changes in beta, and let us proceed with the same type of analysis for the fixed-bias configuration and compare notes.

Fixed-Bias Configuration

The fixed-bias configuration of Fig. 4.71 is from Example 4.1 to permit a comparison of results. Beta was set to 50 using the procedure described above. In this case, we will use a **VIEWPOINT** to read the collector-to-emitter voltage and enable the display of bias currents (using the icon with the large capital **I**). In addition, we will inhibit the display of some bias currents using the icon with the smaller capital **I** and the diode symbol. The final touch is to move some of the currents displayed to clean up the presentation.

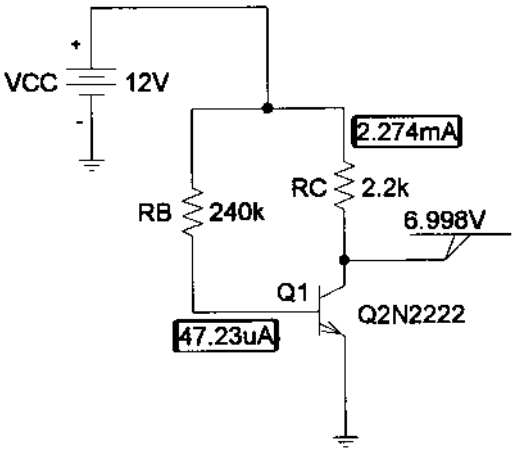


Figure 4.71 Fixed-bias configuration with a β of 50.

A PSpice analysis of the network will result in the levels appearing in Fig. 4.71. These are a close match with the hand-written solution, with the collector voltage at 6.998 V versus 6.83 V, the collector current at 2.274 mA versus 2.35 mA, and the base current at 47.23 μA versus 47.08 μA.

Let us now test the sensitivity to changes in beta by changing to the default value of 255.9. The results appear in Fig. 4.72. Note the dramatic drop in V_C to 0.113 V compared to 6.83 V and the significant rise in I_D to 5.4 mA versus the solution of 2.35 mA. The fixed-bias configuration is obviously very beta-sensitive.

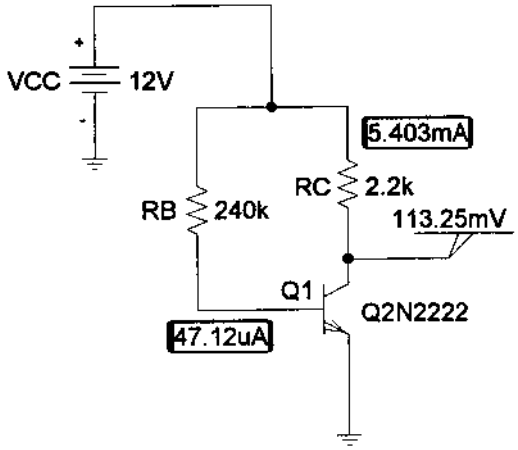


Figure 4.72 Network of Figure 4.71 with a β of 255.9.

PROBLEMS

§ 4.3 Fixed-Bias Circuit

1. For the fixed-bias configuration of Fig. 4.73, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_B.
(f) V_E.

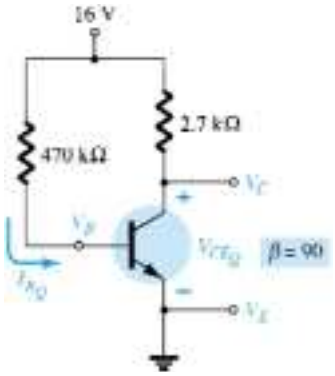


Figure 4.73 Problems 1, 4, 11, 47, 51, 52, 53

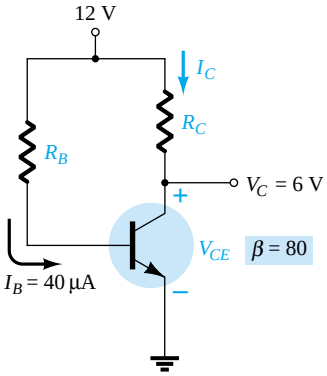


Figure 4.74 Problem 2

2. Given the information appearing in Fig. 4.74, determine:
(a) I_C.
(b) R_C.
(c) R_B.
(d) V_{CE}.

3. Given the information appearing in Fig. 4.75, determine:
(a) I_C.
(b) V_{CC}.
(c) β.
(d) R_B.

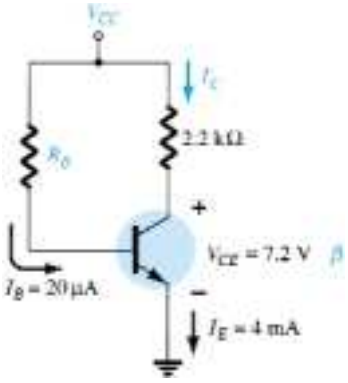


Figure 4.75 Problem 3

4. Find the saturation current ($I_{C_{sat}}$) for the fixed-bias configuration of Fig. 4.73.

*** 5.** Given the BJT transistor characteristics of Fig. 4.76:
(a) Draw a load line on the characteristics determined by $E = 21$ V and $R_C = 3\ k\Omega$ for a fixed-bias configuration.
(b) Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point.
(c) What are the resulting values of I_{C_Q} and V_{CE_Q}?
(d) What is the value of β at the operating point?
(e) What is the value of α defined by the operating point?
(f) What is the saturation ($I_{C_{sat}}$) current for the design?
(g) Sketch the resulting fixed-bias configuration.
(h) What is the dc power dissipated by the device at the operating point?
(i) What is the power supplied by V_{CC}?
(j) Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

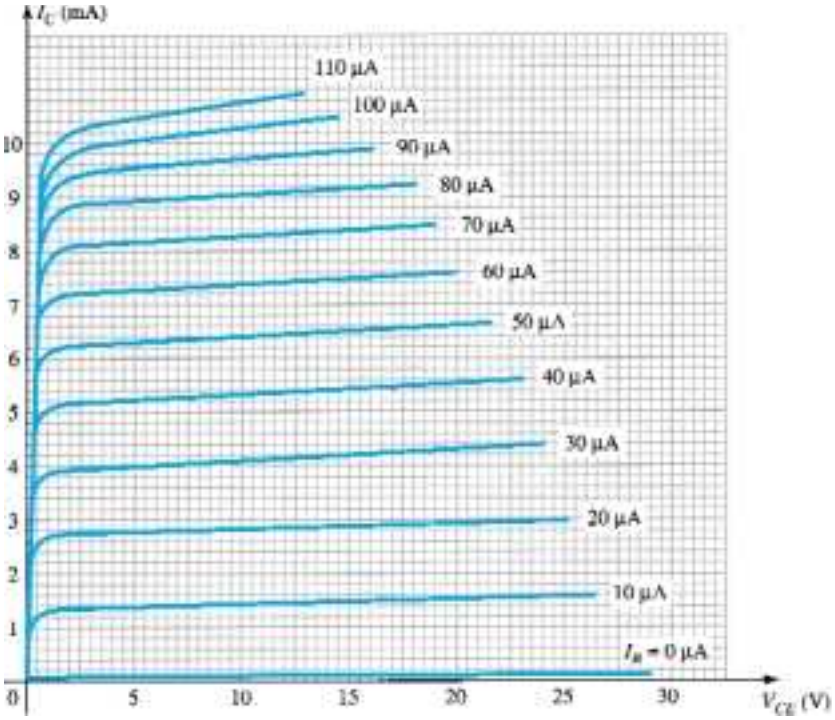


Figure 4.76 Problems 5, 10, 19, 35, 36

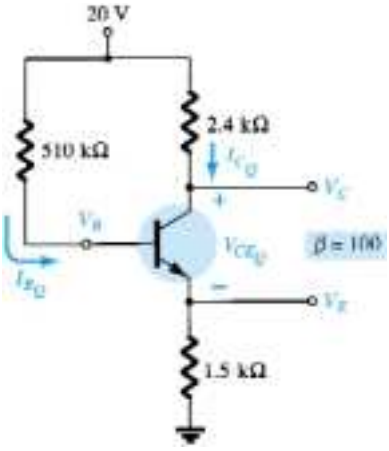


Figure 4.77 Problems 6, 9, 11, 20, 24, 48, 51, 54

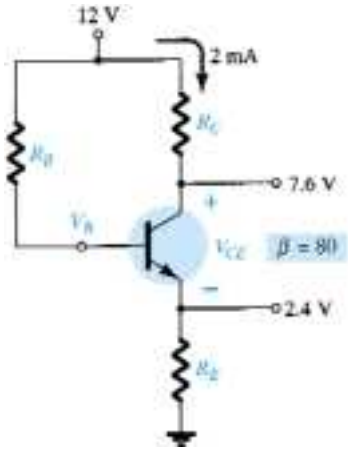


Figure 4.78 Problem 7

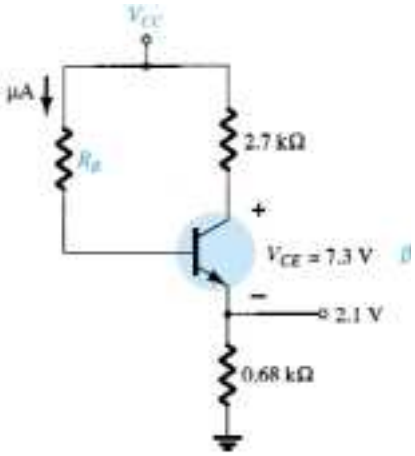


Figure 4.79 Problem 8

§ 4.4 Emitter-Stabilized Bias Circuit

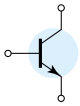
6. For the emitter-stabilized bias circuit of Fig. 4.77, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_B.
(f) V_E.

7. Given the information provided in Fig. 4.78, determine:
(a) R_C.
(b) R_E.
(c) R_B.
(d) V_{CE}.
(e) V_B.

8. Given the information provided in Fig. 4.79, determine:
(a) β.
(b) V_{CC}.
(c) R_B.

9. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.77.

* **10.** Using the characteristics of Fig. 4.76, determine the following for an emitter-bias configuration if a Q-point is defined at $I_{C_Q} = 4$ mA and $V_{CE_Q} = 10$ V.
(a) R_C if $V_{CC} = 24$ V and $R_E = 1.2$ kΩ.
(b) β at the operating point.
(c) R_B.
(d) Power dissipated by the transistor.
(e) Power dissipated by the resistor R_C.



* **11.** (a) Determine I_C and V_{CE} for the network of Fig. 4.73.
(b) Change β to 135 and determine the new value of I_C and V_{CE} for the network of Fig. 4.73.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}} \right| \times 100\%$$

(d) Determine I_C and V_{CE} for the network of Fig. 4.77.
(e) Change β to 150 and determine the new value of I_C and V_{CE} for the network of Fig. 4.77.
(f) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C(\text{part e})} - I_{C(\text{part d})}}{I_{C(\text{part d})}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE(\text{part e})} - V_{CE(\text{part d})}}{V_{CE(\text{part d})}} \right| \times 100\%$$

(g) In each of the above, the magnitude of β was increased 50%. Compare the percent change in I_C and V_{CE} for each configuration, and comment on which seems to be less sensitive to changes in β.

§ 4.5 Voltage-Divider Bias

12. For the voltage-divider bias configuration of Fig. 4.80, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_E.
(f) V_B.

13. Given the information provided in Fig. 4.81, determine:
(a) I_C.
(b) V_E.
(c) V_B.
(d) R_1.

14. Given the information appearing in Fig. 4.82, determine:
(a) I_C.
(b) V_E.
(c) V_{CC}.
(d) V_{CE}.
(e) V_B.
(f) R_1.

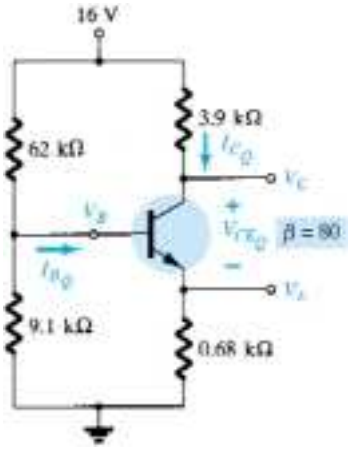


Figure 4.80 Problems 12, 15, 18, 20, 24, 49, 51, 52, 55

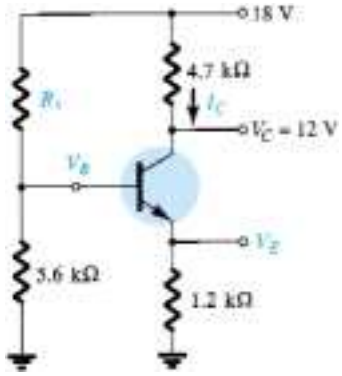


Figure 4.81 Problem 13

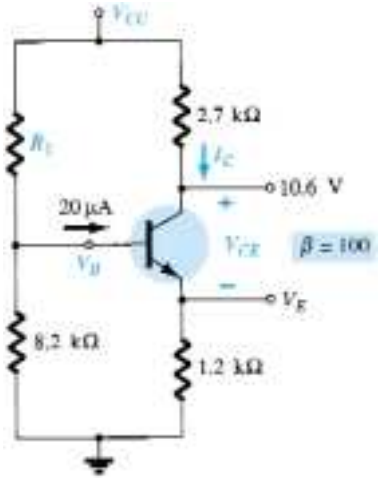


Figure 4.82 Problem 14

15. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.80.

* **16.** Determine the following for the voltage-divider configuration of Fig. 4.83 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
(a) I_C.
(b) V_{CE}.
(c) I_B.
(d) V_E.
(e) V_B.

* **17.** Repeat Problem 16 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?

18. (a) Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} for the network of Problem 12 (Fig. 4.80) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.
(b) Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} using the exact approach.
(c) Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.

* **19.** (a) Using the characteristics of Fig. 4.76, determine R_C and R_E for a voltage-divider network having a Q-point of $I_{C_Q} = 5$ mA and $V_{CE_Q} = 8$ V. Use $V_{CC} = 24$ V and $R_C = 3R_E$.
(b) Find V_E.
(c) Determine V_B.
(d) Find R_2 if $R_1 = 24\ \text{k}\Omega$ assuming that $\beta R_E > 10R_2$.
(e) Calculate β at the Q-point.
(f) Test Eq. (4.33), and note whether the assumption of part (d) is correct.

* **20.** (a) Determine I_C and V_{CE} for the network of Fig. 4.80.
(b) Change β to 120 (50% increase), and determine the new values of I_C and V_{CE} for the network of Fig. 4.80.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left|\frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}}\right| \times 100\%, \qquad \%\Delta V_{CE} = \left|\frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}}\right| \times 100\%$$

(d) Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 11. If not performed, note the solutions provided in Appendix E.
(e) Based on the results of part (d), which configuration is least sensitive to variations in β?

* **21.** (a) Repeat parts (a) through (e) of Problem 20 for the network of Fig. 4.83. Change β to 180 in part (b).
(b) What general conclusions can be made about networks in which the condition $\beta R_E > 10R_2$ is satisfied and the quantities I_C and V_{CE} are to be determined in response to a change in β?

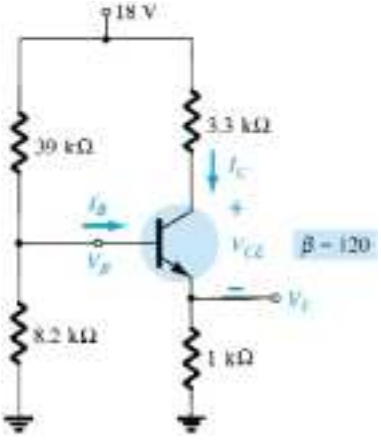


Figure 4.83 Problems 16, 17, 21

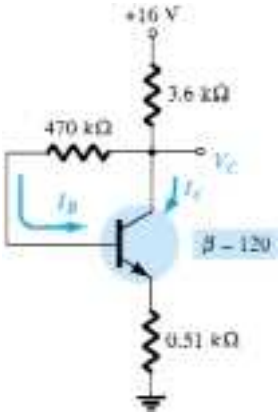


Figure 4.84 Problems 22, 50, 56

§ 4.6 DC Bias with Voltage Feedback

22. For the collector feedback configuration of Fig. 4.84, determine:
(a) I_B.
(b) I_C.
(c) V_C.

23. For the voltage feedback network of Fig. 4.85, determine:
(a) I_C.
(b) V_C.
(c) V_E.
(d) V_{CE}.

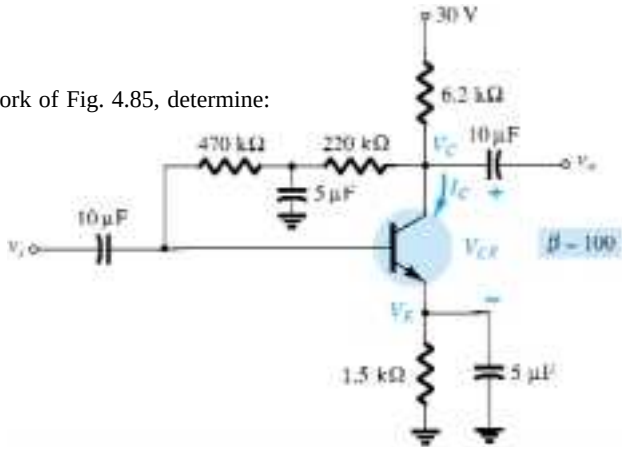
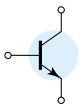


Figure 4.85 Problem 23



* **24.** (a) Determine the level of I_C and V_{CE} for the network of Fig. 4.86.
(b) Change β to 135 (50% increase), and calculate the new levels of I_C and V_{CE}.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}} \right| \times 100\%$$

(d) Compare the results of part (c) with those of Problems 11(c), 11(f), and 20(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in β?

25. Determine the range of possible values for V_C for the network of Fig. 4.87 using the 1-MΩ potentiometer.

* **26.** Given $V_B = 4$ V for the network of Fig. 4.88, determine:
(a) V_E.
(b) I_C.
(c) V_C.
(d) V_{CE}.
(e) I_B.
(f) β.

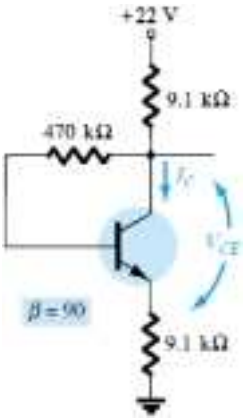


Figure 4.86 Problem 24

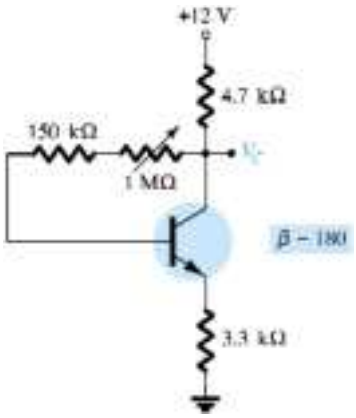


Figure 4.87 Problem 25

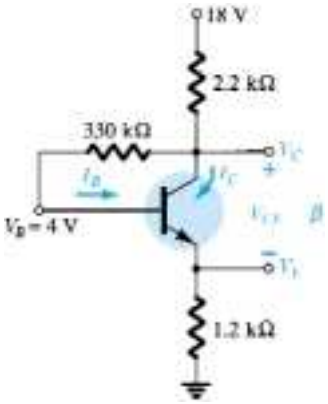


Figure 4.88 Problem 26

§ 4.7 Miscellaneous Bias Configurations

27. Given $V_C = 8$ V for the network of Fig. 4.89, determine:
(a) I_B.
(b) I_C.
(c) β.
(d) V_{CE}.

* **28.** For the network of Fig. 4.90, determine:
(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.

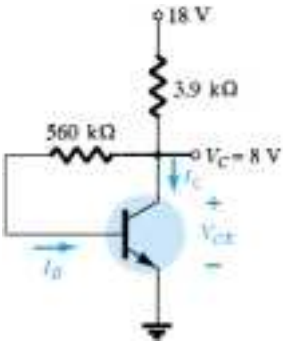


Figure 4.89 Problem 27

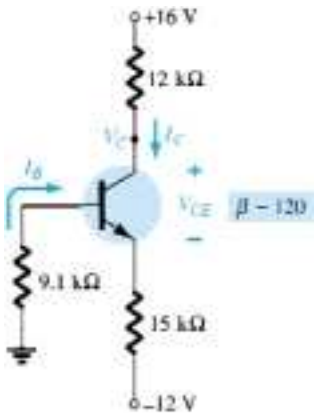
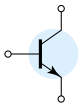


Figure 4.90 Problem 28



* **29.** For the network of Fig. 4.91, determine:
  (a) I_B.
  (b) I_C.
  (c) V_E.
  (d) V_{CE}.

* **30.** Determine the level of V_E and I_E for the network of Fig. 4.92.

* **31.** For the network of Fig. 4.93, determine:
  (a) I_E.
  (b) V_C.
  (c) V_{CE}.

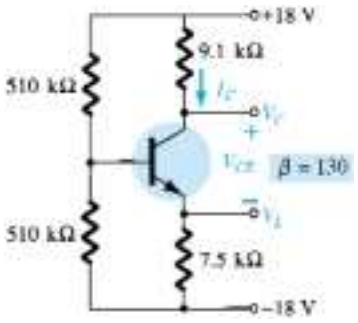


Figure 4.91 Problem 29

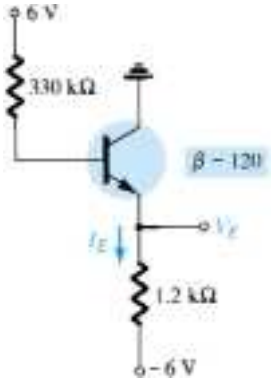


Figure 4.92 Problem 30

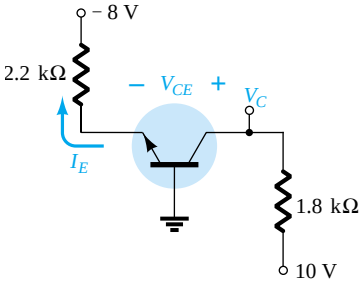


Figure 4.93 Problem 31

§ 4.8 Design Operations

32. Determine R_C and R_B for a fixed-bias configuration if $V_{CC} = 12$ V, $\beta = 80$, and $I_{C_Q} = 2.5$ mA with $V_{CE_Q} = 6$ V. Use standard values.

33. Design an emitter-stabilized network at $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$ and $V_{CE_Q} = \frac{1}{2}V_{CC}$. Use $V_{CC} = 20$ V, $I_{C_{sat}} = 10$ mA, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

34. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of $I_{C_Q} = 4$ mA and $V_{CE_Q} = 8$ V. Choose $V_E = \frac{1}{8}V_{CC}$. Use standard values.

* **35.** Using the characteristics of Fig. 4.76, design a voltage-divider configuration to have a saturation level of 10 mA and a Q-point one-half the distance between cutoff and saturation. The available supply is 28 V, and V_E is to be one-fifth of V_{CC}. The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

§ 4.9 Transistor Switching Networks

* **36.** Using the characteristics of Fig. 4.76, determine the appearance of the output waveform for the network of Fig. 4.94. Include the effects of $V_{CE_{sat}}$, and determine I_B, $I_{B_{max}}$, and $I_{C_{sat}}$ when $V_i = 10$ V. Determine the collector-to-emitter resistance at saturation and cutoff.

* **37.** Design the transistor inverter of Fig. 4.95 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B_{max}}$ and standard resistor values.

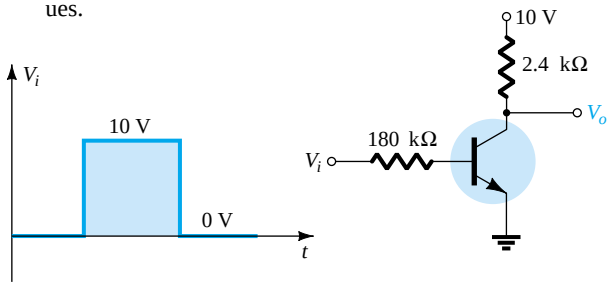


Figure 4.94 Problem 36

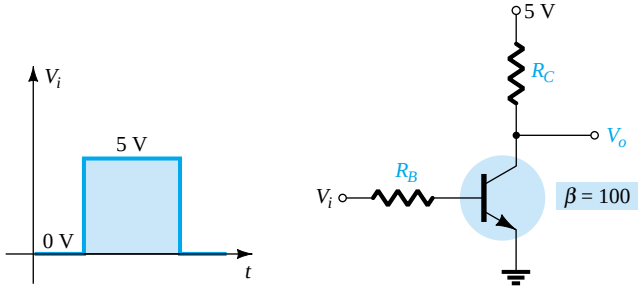


Figure 4.95 Problem 37

38. (a) Using the characteristics of Fig. 3.23c, determine t_{on} and t_{off} at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 11.2.
(b) Repeat part (a) at a current of 10 mA. How have t_{on} and t_{off} changed with increase in collector current?
(c) For parts (a) and (b), sketch the pulse waveform of Fig. 4.56 and compare results.

§ 4.10 Troubleshooting Techniques

* **39.** The measurements of Fig. 4.96 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.

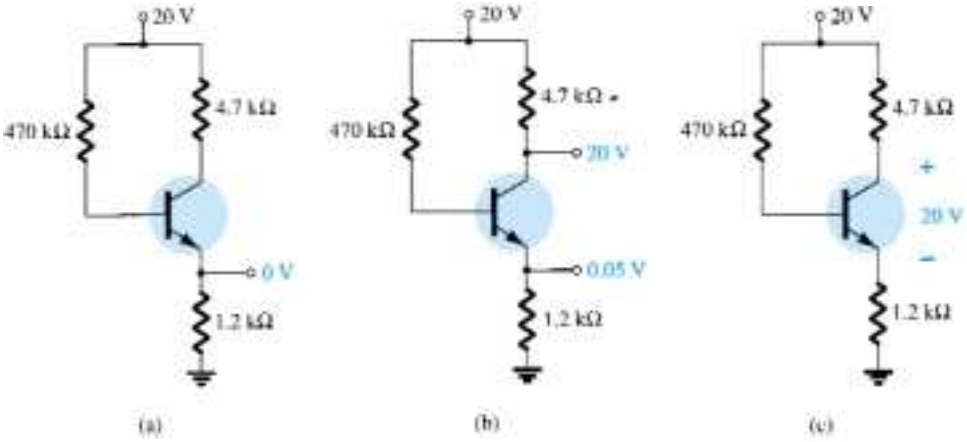


Figure 4.96 Problem 39

* **40.** The measurements appearing in Fig. 4.97 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.

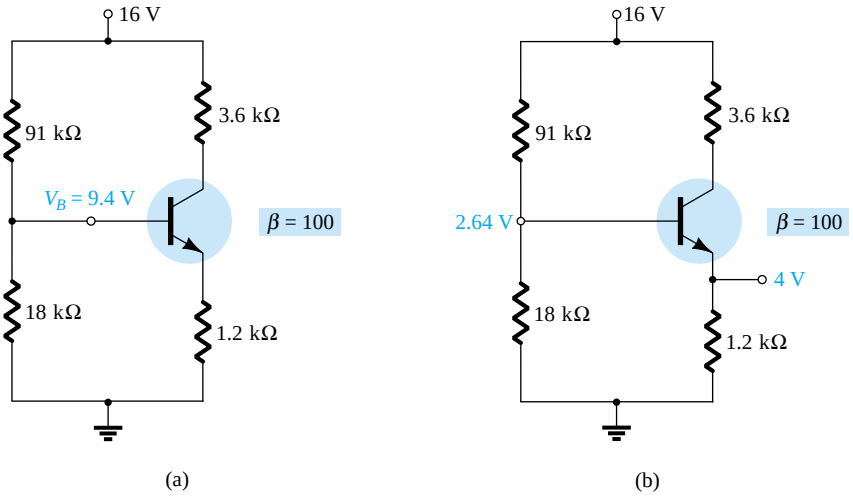


Figure 4.97 Problem 40

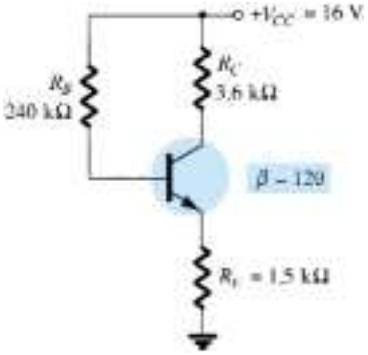


Figure 4.98 Problem 41

41. For the circuit of Fig. 4.98:
(a) Does V_C increase or decrease if R_B is increased?
(b) Does I_C increase or decrease if β is reduced?
(c) What happens to the saturation current if β is increased?
(d) Does the collector current increase or decrease if V_{CC} is reduced?
(e) What happens to V_{CE} if the transistor is replaced by one with smaller β?

42. Answer the following questions about the circuit of Fig. 4.99.
(a) What happens to the voltage V_C if the transistor is replaced by one having a larger value of β?
(b) What happens to the voltage V_{CE} if the ground leg of resistor R_{B_2} opens (does not connect to ground)?
(c) What happens to I_C if the supply voltage is low?
(d) What voltage V_{CE} would occur if the transistor base–emitter junction fails by becoming open?
(e) What voltage V_{CE} would result if the transistor base–emitter junction fails by becoming a short?

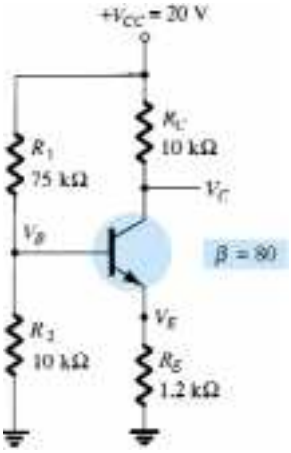


Figure 4.99 Problem 42

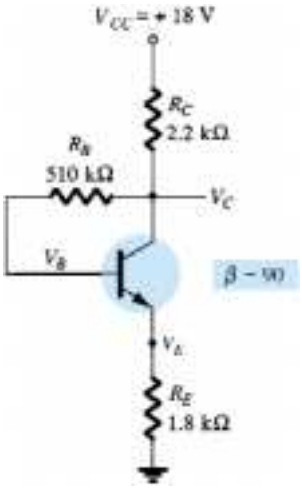


Figure 4.100 Problem 43

* **43.** Answer the following questions about the circuit of Fig. 4.100.
(a) What happens to the voltage V_C if the resistor R_B is open?
(b) What should happen to V_{CE} if β increases due to temperature?
(c) How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
(d) If the transistor collector connection becomes open, what will happen to V_E?
(e) What might cause V_{CE} to become nearly 18 V?

§ 4.11 *PNP* Transistors

44. Determine V_C, V_{CE}, and I_C for the network of Fig. 4.101.

45. Determine V_C and I_B for the network of Fig. 4.102.

46. Determine I_E and V_C for the network of Fig. 4.103.

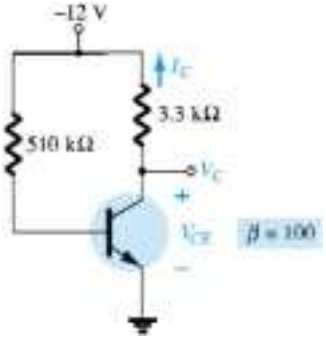


Figure 4.101 Problem 44

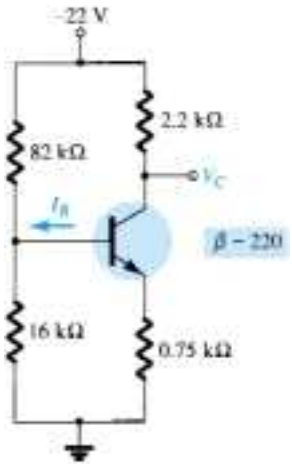


Figure 4.102 Problem 45

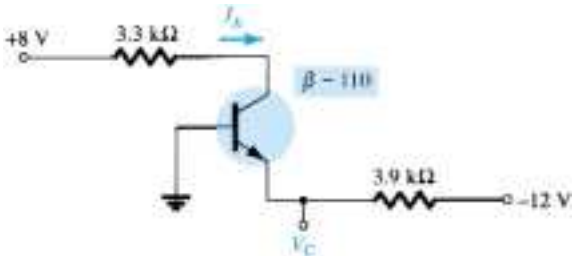
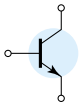


Figure 4.103 Problem 46



§ 4.12 Bias Stabilization

47. Determine the following for the network of Fig. 4.73.
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **48.** For the network of Fig. 4.77, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **49.** For the network of Fig. 4.80, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **50.** For the network of Fig. 4.89, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **51.** Compare the relative values of stability for Problems 47 through 50. The results for Exercises 47 and 49 can be found in Appendix E. Can any general conclusions be derived from the results?

* **52.** (a) Compare the levels of stability for the fixed-bias configuration of Problem 47.
(b) Compare the levels of stability for the voltage-divider configuration of Problem 49.
(c) Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

§ 4.13 PSpice Windows

53. Perform a PSpice analysis of the network of Fig. 4.73. That is, determine I_C, V_{CE}, band I_B.

54. Repeat Problem 53 for the network of Fig. 4.77.

55. Repeat Problem 53 for the network of Fig. 4.80.

56. Repeat Problem 53 for the network of Fig. 4.84.

*Please Note: Asterisks indicate more difficult problems.