

Verifying the diode–capacitor circuit voltage decay

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The voltage on a capacitor discharging through a forward biased diode is calculated from basic equations and is found to be in good agreement with experimental measurements. In contrast to the exponential time decay for a RC circuit, the nonlinear characteristics of the diode result in a nonexponential decay for the diode–capacitor circuit. For a silicon diode the decay is predominantly a logarithmic function of time. © 2003 American Association of Physics Teachers.

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INTRODUCTION

Diodes and capacitors are two of the basic components in electronics. This paper describes the measurement and analysis of the decay of voltage across a capacitor as it discharges through a diode in the forward biased direction. The mathematical form of the decay is derived from fundamental equations for the diode and the capacitor. The measured behavior is found to be in good agreement with the theoretical prediction.

There is inherent academic interest in verifying the predicted behavior of this fundamental electronic circuit. In addition this circuit provides interesting contrast to the well-known exponential decay of voltage for a capacitor discharging through a resistor. In the case of a silicon diode the diode–capacitor circuit is shown to have a voltage decay that is predominantly a logarithmic function of time.

The diode and closely related transdiode have previously been used as convenient sources of semiconductor material for experiments measuring band gap energies and fundamental constants.^{1–3} These make use of the temperature dependence in the basic equation describing the current–voltage characteristics of the diode. This paper uses that equation to predict and verify the behavior of a simple electronic circuit, the diode–capacitor circuit.

This experiment is well suited for beginning students in an electronics course. A brief description of the operation of the experimental electrical circuit is included. Data may be collected using high-end digital storage oscilloscopes or low cost PC-based data acquisition systems. The electrical components are common and inexpensive. The circuits are simple enough that a student with no experience can construct them on a proto-board.

THEORY

The theoretical expression for the decaying voltage across the capacitor is found by setting the rate of change of charge on the capacitor equal to the current through the diode. For the capacitor we have

$$\frac{dQ}{dt} = C \frac{dV}{dt}. \quad (1)$$

For the semiconductor diode we use the standard equation relating its current to its voltage,

$$I = I_0 \left(\exp\left(\frac{qV}{mkT}\right) - 1 \right). \quad (2)$$

The fundamental constants are the elementary charge $q = 1.60 \times 10^{-19}$ C and the Boltzmann constant $k = 1.38 \times 10^{-23}$ J/K. In the ideal case $m = 1$, but for real diodes m ranges from 1 to 2, with silicon diodes having a value close to 2 for small currents (a few milliamps or less). The derivation of this equation is based on a statistical mechanics analysis of the semiconductor PN junction and can be found in many physics or electronics texts.^{4–7} Discussions of the correction factor m can also be found.^{2,7,8} At room temperature the quantity $kT/q = V_T = 25$ mV. I_0 is the reverse saturation current, typically a few to tens of nanoamperes for silicon diodes.

A differential equation is obtained by setting the diode current equal to the negative of the time derivative of the charge on the capacitor,

$$-C \frac{dV}{dt} = I_0 \left(\exp\left(\frac{V}{mV_T}\right) - 1 \right). \quad (3)$$

This can be solved by standard techniques, a table of integrals, and manipulation to give

$$V(t) = -mV_T \ln \left[1 - \left(1 - \exp\left(\frac{-V_i}{mV_T}\right) \right) \exp(-\alpha t) \right], \quad (4)$$

where V_i is the initial voltage at time $t=0$ and $\alpha = I_0/(mV_TC)$. This is the theoretical equation for the decaying voltage on a diode–capacitor circuit. If the temperature, initial voltage, and capacitance are known then the parameters m and I_0 can be found by analyzing the decaying voltage.

It is instructive to consider three time regions for Eq. (4). We start with the condition $\alpha t \ll 1$. Keeping only the first two terms of the expansion of the exponential term containing αt , and upon simplification, Eq. (4) becomes

$$V(t) = -mV_T \ln \left[\exp\left(\frac{-V_i}{mV_T}\right) + \alpha t \left(1 - \exp\left(\frac{-V_i}{mV_T}\right) \right) \right]. \quad (5)$$

The initial voltage will be the voltage drop of a forward biased conducting diode. For a silicon diode the forward voltage drop is typically around 0.6–0.7 V. This is much larger than the quantity mV_T , therefore the second exponential term containing V_i is negligible compared to 1. Equation (5) becomes

$$V(t) = -mV_T \ln \left[\exp\left(\frac{-V_i}{mV_T}\right) + \alpha t \right]. \quad (6)$$

Two cases follow from Eq. (6). For the shortest times, those satisfying $\alpha t \ll \exp[-V_i/(mV_T)]$, Eq. (6) gives the unsurprising result that the voltage is equal to the initial voltage V_i .

For intermediate times, those satisfying $\alpha t \gg \exp[-V_i/(mV_T)]$ yet still satisfying the original condition $\alpha t \ll 1$, Eq. (6) becomes

$$V(t) = -mV_T \ln(\alpha) - mV_T \ln(t). \quad (7)$$

It is convenient to rewrite this in terms of base ten logarithms because many software packages have an option of logarithmic axes on graphs. Using the relationship $\ln(t) \times \log(e) = \log(t)$, Eq. (7) can be rewritten as

$$V(t) = -\frac{mV_T}{\log(e)} \log(\alpha) - \frac{mV_T}{\log(e)} \log(t). \quad (8)$$

This equation graphed versus $\log(t)$ has a constant slope of $-mV_T/\log(e)$. During this range of time the decaying voltage of a silicon diode is a logarithmic function of time.

The third case is to consider all times satisfying $\alpha t \gg \exp[-V_i/(mV_T)]$. Note that this case includes the intermediate time region. The exponential term involving V_i in Eq. (4) can be neglected giving the result

$$V(t) = -mV_T \ln[1 - \exp(-\alpha t)]. \quad (9)$$

Equation (9) has the property that for long times the voltage decays to zero as expected.

The duration of the intermediate time region during which the voltage decay is logarithmic is found from the requirement that $\exp[-V_i/(mV_T)] \ll \alpha t \ll 1$. These two inequalities can define two transition times between the time regions. As an example, for a silicon diode we take V_i to be a forward voltage drop of 0.6 V and m to be 2 giving $\exp(-0.6/0.05) = 6.1 \times 10^{-6}$. Thus there are about five orders of magnitude of time during which the decay is approximately logarithmic as the quantity αt increases from 6.1×10^{-6} to 1. The transition from the early time region (voltage is constant) to the intermediate time region (voltage decays logarithmically) occurs at

$$t = \frac{1}{\alpha} \exp\left(\frac{-V_i}{mV_T}\right) = \frac{mV_T C}{I_0} \exp\left(\frac{-V_i}{mV_T}\right). \quad (10)$$

The transition from the intermediate time region to the final time region where the decay is no longer logarithmic occurs at

$$t = \frac{1}{\alpha} = \frac{mV_T C}{I_0}. \quad (11)$$

Note that the transition times are proportional to the capacitor value. Calculation of the expected transition times can help determine experimental requirements such as sampling rate and duration. A capacitance value can be chosen to adjust the time scale of the experiment to be appropriate for available equipment.

EXPERIMENT AND RESULTS

The components are basic, inexpensive, and readily available. The electrical circuit shown in Fig. 1 is simple enough to be constructed by a beginner. It requires ± 15 and $+5$ volt power supplies. The diode-capacitor circuit is the 1N4148 silicon diode and the capacitor C_1 .

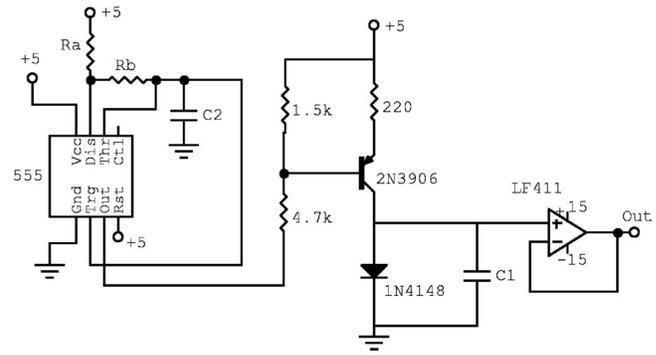


Fig. 1. Schematic for repetitive discharge of the diode-capacitor circuit (1N4148 diode and C_1). Components include 555 timer, 2N3906 PNP transistor, and LF411 op amp.

Capacitor C_1 is quickly charged by current from the PNP transistor (2N3906). The biasing of the base of the PNP and the 220- Ω resistor at its emitter sets a constant current of about 2 mA during the charging phase. The capacitor voltage increases until it reaches the voltage appropriate for a diode conducting the entire charging current. At 2 mA a typical silicon diode has a voltage drop of about 0.6–0.7 V. This is the initial voltage V_i for the decay. This voltage is easily measured with an oscilloscope during the charging phase.

It is important to realize that the decaying capacitor voltage must be detected with a high impedance device because the effective resistance of the diode becomes very high as the voltage approaches zero. This is the purpose of the op amp functioning as a unity gain buffer. JFET input op amps, such as the LF411, have input resistances of $10^{12} \Omega$. Standard 1- or 10-M Ω oscilloscope probes should not be connected directly to the capacitor voltage. Recording devices such as oscilloscope probes or inputs to PC-based data acquisition cards should be connected to the output of the op amp.

It is convenient to have the capacitor repeatedly charge and discharge. The popular and versatile 555-timer chip is used in its astable configuration to periodically turn on the PNP transistor to quickly charge the capacitor. This occurs when the 555 output goes low for a time $0.693R_B C_2$ pulling the base of the PNP down to about 4 V. The PNP transistor is turned off when the 555 output goes high for a time $0.693(R_A + R_B)C_2$. During this time the capacitor C_1 discharges through the diode. As an example, using $R_A = 680 \text{ k}\Omega$, $R_B = 1 \text{ k}\Omega$, and $C_2 = 2.2 \mu\text{f}$ gives a charging time of 1.5 ms and a discharging time of 1 s. The rising edge of the 555 output provides a convenient trigger marking the beginning of the decay.

Figure 2 shows the voltage versus time for a 0.1- μf capacitor discharging through the 1N4148 diode. Figure 3 shows the same data plus data for 0.01- and 0.001- μf capacitors plotted versus the logarithm of time, $\log(t)$. Data were collected with a digitizing storage oscilloscope (HP 54501A). Data sets collected with different sampling rates were combined in order to span six decades of time. Analysis of the data provides values for the parameters m and I_0 . In all three cases the initial voltage was 620 mV. Also shown, by the large open symbols, are the voltages for each capacitor calculated using Eq. (4). There are only two free parameters in this equation, m and I_0 . Parameter m determines the slope of the linear decline versus $\log(t)$ and I_0 determines the vertical offset. Thus it is easy to manually find best-fit pa-

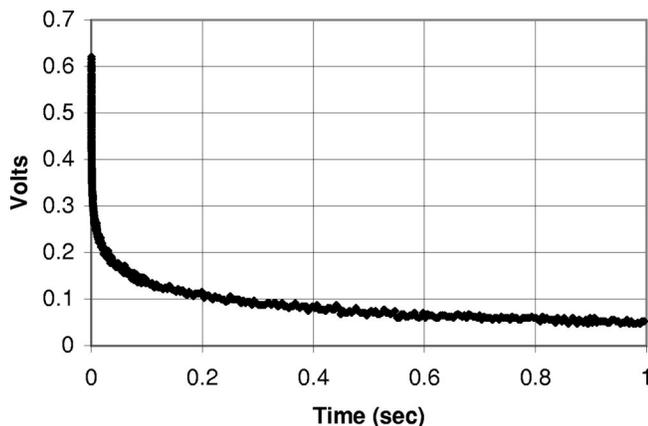


Fig. 2. Measured voltage decay for a $0.1\text{-}\mu\text{f}$ capacitor through a 1N4148 diode. Initial voltage is 0.62 V.

rameters for m and I_0 . The three data curves were simultaneously fit by Eq. (4), with best-fit parameters $m=1.90 \pm 0.05$ and $I_0=2.5 \pm 0.5$ nA.

Another simple circuit, shown in Fig. 4, is used to make an independent measurement of the reverse saturation current I_0 of the diode. The diode is reverse biased and the current passes through a $10\text{-M}\Omega$ resistor generating a voltage that is detected by the high input impedance op amp used as a unity gain buffer. A FET input op amp with low offset voltage should be used such as the LF411. In this configuration a current of 1 nA generates a voltage of 10 mV. Figure 5 shows a graph of the reverse current as a function of the reverse-biased voltage.

The initial rapid rise in current in Fig. 5 is what is of interest in determining I_0 . The slower rise apparent for voltages from 5 to 35 V is attributed to leakage current. Examination of Eq. (2) shows that when the reverse voltage is many times V_T , the saturation current has been reached because the exponential term is much less than unity. Further increase in current is due to leakage current which is not included in the derivation of Eq. (2). Examination of Fig. 5 suggests that when this leakage current is extrapolated back

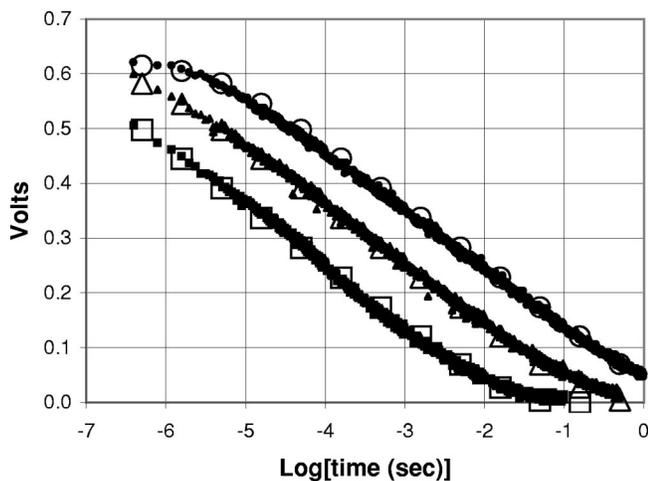


Fig. 3. Measured voltage decay (small closed symbols) vs $\log(t)$ and predicted decay (large open symbols) using the exact solution, Eq. (4), and parameters given in text. Capacitor values from left to right, 0.001, 0.01, and $0.1\ \mu\text{f}$.

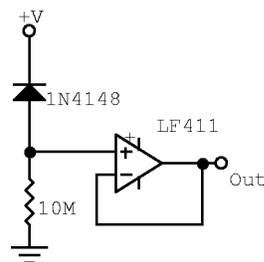


Fig. 4. Schematic for measuring reverse biased current through the diode. The voltage $+V$ varies from 0 to $+35$ V. A current of 1 nA will generate a 10 mV output.

to 0 V the saturation current is around 1.5–2.5 nA. This is consistent with the 2.5 nA found from the analysis of the diode–capacitor circuit’s decaying voltage.

DISCUSSION

Figure 2 shows the voltage decay for a $0.1\text{-}\mu\text{f}$ capacitor through a 1N4148 diode. The initial drop is quite fast as expected for a forward biased diode. However as the voltage drops to a few tenths of a volt, the diode’s resistance [the inverse of the slope of Eq. (2)] increases significantly. As a result the voltage decay slows as time goes on. For this reason it is more enlightening to plot the voltage versus $\log(t)$ as shown in Fig. 3.

Figure 3 shows data for the voltage versus $\log(t)$ for capacitor values of 0.1, 0.01, and $0.001\ \mu\text{f}$ discharging through a 1N4148 diode. Also shown are the predicted voltages using Eq. (4) with the values $m=1.9$ and $I_0=2.5$ nA. These values agree well with the finding that m is close to 2 and I_0 is in the nanoampere range for silicon diodes.^{6,7} It is also consistent with the reverse saturation current obtained by reverse biasing the diode.

In Fig. 3 note how well the calculated voltage follows the data through the three time regions discussed in the Theory section. The only data set that clearly shows the early time region where the voltage is nearly constant is the $0.1\text{-}\mu\text{f}$ capacitor. Transitions between the regions are predicted to occur at the transition times given by Eqs. (10) and (11). The predicted transition times can be compared to the behavior of the data in Fig. 3. Using $m=1.9$, $I_0=2.5$ nA, $V_T=25$ mV, $V_i=620$ mV, and $C=0.1, 0.01,$ and $0.001\ \mu\text{f}$, we predict

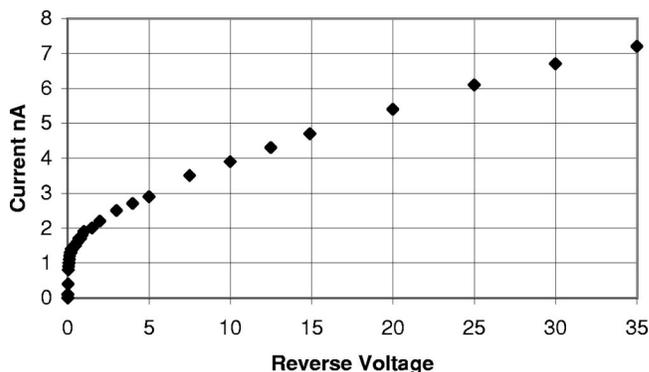


Fig. 5. Measured current vs reverse biased voltage for 1N4148 diode. Note the initial rapid rise followed by the slower increase.

early-to-intermediate region transition times of 0.04, 0.4, and 4 μs , and intermediate-to-final region transition times of 0.02, 0.2, and 2 s.

The early-to-intermediate transition is from the region of constant initial voltage (0.62 V) to the region of logarithmic decay. The predicted transition times of 0.4 and 4 μs for the 0.01- and 0.1- μf capacitors agree well with the data in Fig. 3. For the 0.001- μf capacitor the predicted transition time of 0.04 μs is consistent with the data since the voltage must have dropped from 0.62 to 0.5 V prior to the first measurement at 0.4 μs . The intermediate-to-final transition is from the region of logarithmic decay to the region of final decay to zero. The predicted transition times of 0.02 and 0.2 s for the 0.001- and 0.01- μf capacitors agree well with the data in Fig. 3. For the 0.1- μf capacitor the predicted transition time of 2 s is consistent with the data since the voltage must drop to zero.

Figure 3 also shows that the voltage decay is logarithmic for about 5 decades of time as predicted for a silicon diode in the Theory section. Equation (8) shows that a plot of voltage versus $\log(t)$ will give a straight line with slope $-mV_T/\log(e)$ and that the offset is determined by I_0 through its appearance in $-mV_T \ln(\alpha)/\log(e)$. Data are easily analyzed by finding the value of m that gives the correct slope, then the value of I_0 that gives the proper offset. For example, examination of Fig. 3 or 6 shows that during the logarithmic phase the voltage drops 0.11 V per decade. Thus $m = 0.11 \times \log(e)/0.025 = 1.9$, agreeing with the finding in the Experiment and Results section. Figure 6 shows the data and the calculated decays using Eq. (8) with the same parameters used for Fig. 3. The straight-line portion of the data is seen to follow the lines predicted from Eq. (8).

It is instructive to compare the diode-capacitor circuit's voltage decay to the well-known RC decay. The exponential decay for the RC circuit is a result of the resistor's linear relationship between current and voltage. The nonlinear characteristics of the diode [Eq. (2)] result in nonexponential decay of the voltage. This difference is easy to demonstrate experimentally by replacing the diode with a resistor and repeating the analysis trying both an exponential decay and Eq. (4).

By choosing larger values for C_1 the voltage decay can be made quite long making it possible to use relatively slow data acquisition systems. Figure 3 and Eqs. (10) and (11) demonstrate that the time scale of the decay is proportional to the capacitance. With a 10- μf capacitor a low-end data collection system collecting 100 samples per second will be able to generate a curve like the 0.001- μf capacitor in Figs. 3 and 6, but shifted to the right by four time decades. In this case data collection should extend to at least 100 s.

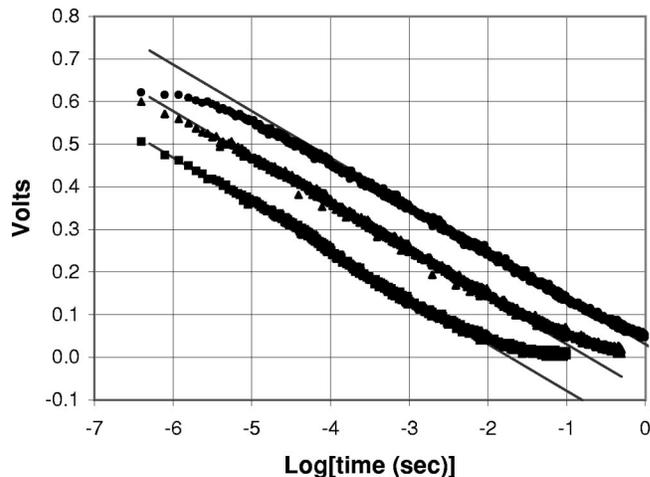


Fig. 6. Measured voltage decay (small closed symbols) vs $\log(t)$ and predicted decay (lines) using the logarithmic approximation, Eq. (8), and parameters given in text. Capacitor values from left to right, 0.001, 0.01, and 0.1 μf .

CONCLUSION

The basic equations for a capacitor and a diode were used to derive an equation for the time-dependent decay of voltage across a diode-capacitor circuit. Measurements were performed and found to be in good agreement with the predictions. Parameters found from the analysis are in good agreement with known values for silicon diodes. For a silicon diode the diode-capacitor circuit's voltage was found to have a predominantly logarithmic time decay. An instructive comparison can be made with the exponential decay of a RC circuit. This experiment is low cost and appropriate for beginning students in an electronics course for scientists.

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